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06MAT41

Fourth Semester B.E. Degree Examination, December 2012
Engineering Mathematics – IV

Time: 3 hrs.

Max. Marks:100

Note: Answer FIVE full questions, selecting at least TWO questions from each part.

PART – A

- 1 a. Given that $\frac{dy}{dx} = x^2 + y^2$ and $y(0) = 1$, to find an approximate value of y at $x = 0.1$ and $x = 0.2$ by Taylor's series method. (06 Marks)
- b. Using Euler's modified method, solve for y at $x = 0.1$ if $\frac{dy}{dx} = \frac{y-x}{y+x}$, $y(0) = 1$, carryout three modifications. (07 Marks)
- c. Given $\frac{dy}{dx} = (1+y)x^2$ and $y(1) = 1$, $y(1.1) = 1.233$, $y(1.2) = 1.548$, $y(1.3) = 1.979$, determine $y(1.4)$ by Adams – Bash forth method. (07 Marks)
- 2 a. Show that an analytic function with constant modulus is constant. (06 Marks)
- b. Find the analytic function $f(z) = u + iv$, if $u = e^{-x} \{(x^2 - y^2) \cos y + 2xy \sin y\}$ (07 Marks)
- c. Find the bilinear transformation which maps the points $z = 1, i, -1$ into the points $w = i, 0, -i$ and hence find the image $|z| < 1$. (07 Marks)
- 3 a. Using the Cauchy's integral formula, to evaluate $\int_c \frac{\cos \pi z^2}{(z-1)(z-2)} dz$ where $c : |z| = 3$. (06 Marks)
- b. Obtain the Laurent's series for the function $f(z) = \frac{z^2 - 1}{z^2 + 5z + 6}$ in the regions i) $2 < |z| < 3$
ii) $|z| > 3$. (07 Marks)
- c. Determine the poles of $\frac{z^2}{(z-1)^2(z+2)}$ and the residues at each pole. (07 Marks)
- 4 a. Prove that $e^{\frac{x}{2}(t-\frac{1}{t})} = \sum_{n=-\infty}^{\infty} t^n J_n(x)$. (06 Marks)
- b. Show that $J_n(x) = \frac{x}{2n} \{J_{n+1}(x) + J_{n-1}(x)\}$ (07 Marks)
- c. Explain the polynomial $2x^3 - x^2 - 3x + 2$ in terms of Legendre's polynomials. (07 Marks)

PART – B

- 5 a. Fit a straight line to the following data: (06 Marks)

x:	0	1	2	3	4
y:	1.0	1.8	3.3	4.5	6.3

- 5 b. Prove that $\tan \theta = \left(\frac{1-r^2}{r} \right) \frac{\sigma_x \sigma_y}{\sigma_x^2 + \sigma_y^2}$, where γ , σ_x , σ_y have their usual meanings and explain the significance of $r = \pm 1$ and $r = 0$. (07 Marks)
- c. A certain problem is given to four students for solving. The probability of their solving the problem are $\frac{1}{2}$, $\frac{1}{3}$, $\frac{1}{4}$ and $\frac{1}{5}$ respectively. Find the probability that the problem is solved. (07 Marks)
- 6 a. The probability density function $P(x)$ of a continuous random variables is given by, $P(x) = y_0 e^{-|x|}$, $-\infty < x < \infty$, prove that $y_0 = \frac{1}{2}$. Find the mean and variance of the distribution. (06 Marks)
- b. Derive the mean and variance of the binomial distribution. (07 Marks)
- c. If x is an exponential variate with mean 4, evaluate i) $P(0 < x < 1)$ ii) $P(x > 2)$ and iii) $P(-\infty < x < 10)$. (07 Marks)
- 7 a. Define the terms: i) Null hypothesis ii) Level of significance and iii) Confidence limits. (06 Marks)
- b. A sugar factory is expected to sell sugar in 100 kg bags. A sample of 144 bags taken from a day's output shows the average and S.D. of weights of these bags as 99 and 4 kg respectively. Can we conclude that the factory is working as per standards? (Table value of $z = 1.96$ at 5% Log) (07 Marks)
- c. The following table gives the number of aircraft accidents that occurred during the various days of the week. Find whether the accident are uniformly distributed over the week. ($X_{0.05}^2 = 9.41$ for 4 d.f.) (07 Marks)

Day	Sun	Mon	Tue	Wed	Thu	Fri	Sat	Total
No. of accident	14	16	8	12	11	9	14	84

- 8 a. The joint probability distribution for the following table:

x \ y	2	3	4
1	0.06	0.15	0.09
2	0.14	0.35	0.21

Determine the marginal distribution of x and y and verify that x and y are independent variables. (06 Marks)

- b. Find the fixed probability vector of the following regular stochastic matrix.

$$A = \begin{bmatrix} \frac{1}{2} & \frac{1}{4} & \frac{1}{4} \\ \frac{1}{2} & 0 & \frac{1}{2} \\ 0 & 1 & 0 \end{bmatrix}$$

(07 Marks)

- c. Define the following terms:

i) Regular state ii) Periodic state iii) Recurrent state and iv) Transient state.

(07 Marks)

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06ES42

Fourth Semester B.E. Degree Examination, December 2012
Micro Controllers

Time: 3 hrs.

Max. Marks:100

**Note: Answer FIVE full questions, selecting
at least TWO questions from each part.**

PART – A

- 1 a. Give the comparison between microprocessor and microcontroller. (05 Marks)
b. With diagram, explain the architecture of 8051. (10 Marks)
c. Give the bit and byte addresses of special function registers available in 8051. (05 Marks)
- 2 a. With example, explain the following 8051 instructions:
i) CJNE; ii) DAA; iii) XCHD; iv) PUSH; v) SUBB. (10 Marks)
b. A byte is stored in internal RAM location 40h write an ALP to count the number of 1's present in the byte and store the count in external memory location 5000h. (06 Marks)
c. Explain bit level logical instructions of 8051. (04 Marks)
- 3 a. With example, explain the sequence of events that occur when a subroutine is executed. (05 Marks)
b. Explain jump instructions with reference to range. Give the diagram. (06 Marks)
c. Give the sequence of events that occur when a interrupt signal is generated. Also explain the role of bits in IE and IP SFR's in the process of interrupt. (09 Marks)
- 4 a. Write an 8051C program to toggle all bits of Port 0 and Port 2 such that Port 0 displays the complement of Port 2 continuously with a delay of 250 m sec. (05 Marks)
b. Write a 'C' program to send out the value 44h serially one bit at a time via P1.0. The MSB should go out first. (05 Marks)
c. Write an 8051 C program to monitor bit P 2.5 continuously. If it is high send 11h to P1 otherwise send FFh to P0. (05 Marks)
d. Give the different data types in 'C' with range. (05 Marks)

PART – B

- 5 a. Explain with diagram, different modes of operation of timers/counters in 8051. (10 Marks)
b. Write an ALP to generate square wave with ON time of 10 m sec and OFF time of 3 m sec on Port P1.0. Assume XTAL of 22 MHz. Use time 0 in mode 1. (05 Marks)
c. Assume that 60 Hz external clock is applied to To. Write a 'C' program for counter 0 in mode 2 to display seconds and minutes on P1 and P2. (05 Marks)
- 6 a. Explain RS 232 hand shaking signals. (05 Marks)
b. Explain the steps to
i) Transfer character bytes serially
ii) Receive the data serially. (10 Marks)
c. Explain the methods to increase baud rate of data transfer in 8051. (05 Marks)

- 7 a. Explain with diagram, how the sampling of low level triggered interrupt and edge triggered interrupt is done XTAL = 11.0592 MHz. (06 Marks)
- b. Generate a square wave from all pins of Port 0 having half the frequency of signal applied to INTO pin of 8051. Use an ALP. (05 Marks)
- c. What is the difference between interrupts and polling? Explain. (05 Marks)
- d. Explain RI and TI interrupts. (04 Marks)
- 8 a. With diagram, explain how to interface 4×4 matrix keyboard to 8051. Give the algorithm. (10 Marks)
- b. Give a scheme to interface ADC with 8051. Also write a program to do the conversion. (10 Marks)

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06ES43

Fourth Semester B.E. Degree Examination, December 2012
Control Systems

Time: 3 hrs.

Max. Marks:100

Note: 1. Answer FIVE full questions atleast
TWO questions from each part.

2. Semi-log sheets may be provided for Q7(b).

PART - A

- 1 a. Define 'control system'. Draw the basic block diagram of a control loop giving all the relevant details. (04 Marks)
- b. Distinguish briefly between open loop and closed loop systems ; linear and non – linear systems ; and time –variant and time – invariant systems. (06 Marks)
- c. For the mechanical translational system shown in Fig. Q1(c), draw the mechanical network ; write the mechanical and electrical differential equation and obtain the force – voltage analogy. (10 Marks)

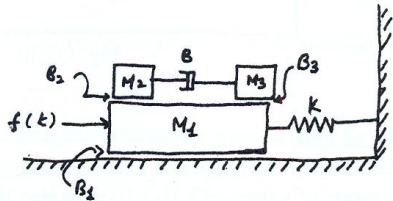


Fig. Q1(c)

- 2 a. Using block diagram reduction technique, find the overall transform function of the system represented by the block diagram shown in Fig. Q2(a) (10 Marks)

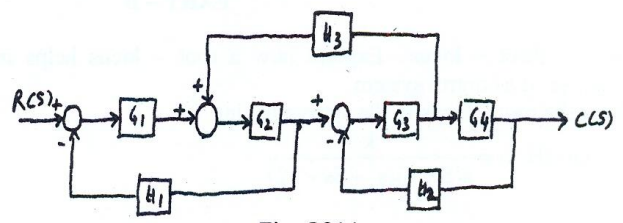


Fig. Q2(a)

- b. Using Mason's gain formula, obtain x_8/x_1 for the signal flow graph shown in Fig. Q2(b). (10 Marks)

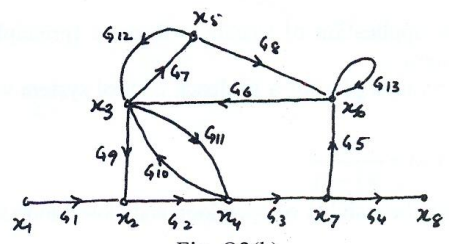


Fig. Q2(b)
1 of 3

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg. 42+8 = 50, will be treated as malpractice.

- 3 a. Draw the typical time domain in response of an underdamped second order system to a unit step input and define the various time domain performance parameters indicating the same on the diagram. (10 Marks)
- b. Fig. Q3(b) shows a system employing proportional plus error-rate control. Determine the value of the error-rate factor k_e so that the damping ratio is 0.5. Determine the values of settling time k_s , maximum overshoot M_p , and steady state error e_{ss} for a unit ramp input with and without error – rate control. Comment upon the effect of error – rate control on system dynamics. (10 Marks)

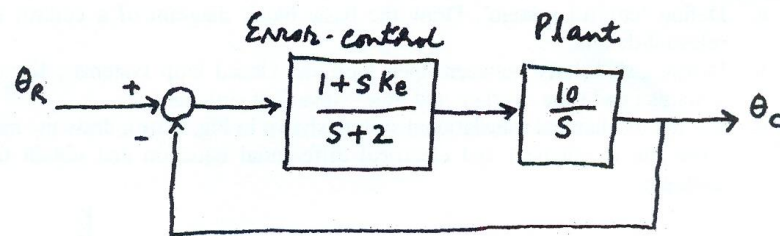


Fig. Q3(b)

- 4 a. Explain BIBO and Zero – input stability. (04 Marks)
- b. What are the benefits of feedback in a control system? (04 Marks)
- c. Determine the range of values of k ($k \geq 0$) such that the characteristic equation $s^3 + 3(k + 1)s^2 + (7k + 5)s + (4k + 7) = 0$ has roots more negative than $s = -1$. (12 Marks)

PART – B

- 5 a. Define ‘Root – locus’. Explain how a root – locus helps in stapling the time domain response of a control system. (08 Marks)
- b. Draw the root – locus fo the system having

$$G(s)H(s) = \frac{k}{s(s+4)(s^2+8s+32)}$$

As k is varied from 0 to ∞ . Show all the steps involved in drawing the root – locus and also mention all the details on the diagram. Comment on stability of the system. (12 Marks)

- 6 a. Explain the application of Cauchy’s theorem (principle of arrangement) used in Nyquist stability criterion. (08 Marks)
- b. Construct Nyquist plot for a feedback control system whose loop transfer function is given by

$$G(s)sH(s) = \frac{5}{s(1-s)}$$

Comment on the stability of open loop and closed loop system. (12 Marks)

- 7 a. Derive the expression for resonance peak (M_r) for a second order system whose closed loop transfer function is

$$\frac{C(s)}{R(s)} = \frac{w_n^2}{s^2 + 2sw_n s + w_n^2} \quad (08 \text{ Marks})$$

- b. A system has the loop transfer function

$$G(s)H(s) = \frac{k}{s(1+s)(1+0.1s)(1+0.01s)}$$

- i) Find the gain margin and phase margin for $k = 1$
 ii) Determine the values of k so that the gain margin is +10 dBs and phase margin is +25°. (12 Marks)

- 8 a. Draw a comparison between the transfer function method of analysis and state space variables approach. (06 Marks)
 b. Write the advantages and disadvantages of state space representation of transfer function using phase variables. (06 Marks)
 c. Obtain the Jordan canonical form of presentation for the transfer function

$$G(s) = \frac{s+3}{s^3 + 9s^2 + 24s + 20}$$

Also draw the corresponding signal flow graph. (08 Marks)

PART - B

- 5 a. Find the discrete time Fourier transformation of the time domain sequence $x[n] = \alpha^n u[n]$ and plot the magnitude and phase spectrum for the values of α (i) $\alpha = 0.5$, (ii) $\alpha = 0.9$. (08 Marks)
- b. The DTFT of a time domain sequence is defined as

$$X(e^{j\Omega}) = \begin{cases} 1 & |\Omega| < W \\ 0 & W \leq |\Omega| < \pi \end{cases}$$



Find its IDTFT and plot $x[n]$.

(06 Marks)

- c. For a moving average spectrum is described by $y[n] = \frac{1}{2}[x[n] + x[n-1]]$. Find its frequency response $H(e^{j\Omega})$ and plot amplitude and spectrum. (06 Marks)

- 6 a. The input to a discrete time system is given by $x[n] = \cos\left(\frac{\pi}{8}n\right) + \sin\left(\frac{3\pi}{4}n\right)$. Use the DTFT to find the output of the system $y[n]$, if the impulse response is given by

i) $h[n] = \frac{\sin\left(\frac{\pi}{4}n\right)}{\pi n}$ ii) $h[n] = (-1)^n \frac{\sin\left(\frac{\pi}{2}n\right)}{\pi n}$ (10 Marks)

- b. Consider the continuous time domain analog signal given by $x(t) = 3 \cos 100\pi t$.
- Determine the minimum sampling rate required to avoid aliasing.
 - Suppose the signal is sampled at $F_s = 200$ Hz, find the corresponding discrete time sequence.
 - Suppose the signal is sampled at $F_s = 75$ Hz, find the corresponding discrete time sequence.
 - What is the frequency $0 < F < \frac{F_s}{2}$ of a sinusoid that yields samples identical to those obtained in part (iii)? (10 Marks)

- 7 a. Define z-transformation and its inverse. State the important condition for the existence of the z transformation using ROC. (05 Marks)
- b. Explain how the ROC in the z domain can change if the corresponding time domain sequences can be left sided, right sided and two sided, while the length can be of finite or infinite duration. (05 Marks)

- c. Give that $x[n] = \begin{cases} a^n & \text{for } 0 \leq n \leq N-1 \\ 0 & \text{otherwise} \end{cases}$. Let $a = 0.5$, $N = 8$. Find $z\{x[n]\}$ using:

- i) Direct evaluation of finite sum of $X[z]$, ii) Sample shifting property of $X[z]$.
Plot its poles and zeros, ROC, and comment on stability. (10 Marks)

- 8 a. A causal LTI system is characterized by having input sequence $x[n] = \left(-\frac{1}{3}\right)^n u[n]$ and

output sequence $y[n] = 3(-1)^n u[n] + \left(\frac{1}{3}\right)^n u[n]$. Determine its transfer function impulse response and difference equation representation. (10 Marks)

- b. Solve the following difference equation using unilateral z transforms and find time domain solution:

i) $y[n+2] - 3y[n+1] + 2y[n] = 4^n u[n]$ for $y[0] = 0$, $y[1] = 1$.

ii) $y[n] + y[n-2] = \delta[n]$ zero initial conditions. (10 Marks)

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06EC45

Fourth Semester B.E. Degree Examination, January 2013
Fundamentals of HDL

Time: 3 hrs.

Max. Marks:100

Note: Answer FIVE full questions, selecting at least TWO questions from each part.

PART – A

1. a. Explain how data types are classified in HDL. Mention the advantages of VHDL data types over verilog. (06 Marks)
b. Explain composite and access data types with an example for each. (08 Marks)
c. Discuss the logical operators in VHDL. (06 Marks)
2. a. Explain signal declaration and signal assignment statements with relevant examples. (06 Marks)
b. Write a dataflow description (in both VHDL and verilog) for a full-adder with active high enable. (08 Marks)
c. Write HDL codes for 2×2 bit combinational array multiplier. (06 Marks)
3. a. Write behavioral description of a half-adder in VHDL and verilog with propagation delay of 5 nsec. Discuss the important features of their description in VHDL and verilog. (08 Marks)
b. Explain the execution of process statement. (02 Marks)
c. Write VHDL code for a D latch using variable assignment statement and signal assignment statements. With simulation waveforms clearly distinguish between the two statements. (10 Marks)
4. a. What is binding? Discuss the binding between library and components. (08 Marks)
b. Write the HDL description of 2:1 multiplexer with active low enable in VHDL/verilog using structural style. (12 Marks)

PART – B

5. a. Explain the following syntax with examples:
i) Procedure
ii) Task
iii) Function. (06 Marks)
b. Write VHDL/verilog code to convert a fractional binary to real number using procedures/tasks. (08 Marks)
c. Describe all file processing tasks in verilog. (06 Marks)

- 6 a. What is the necessity of mixed type description? (04 Marks)
 b. Describe the development of HDL code for an ALU and write VHDL/verilog code for an ALU shown below.

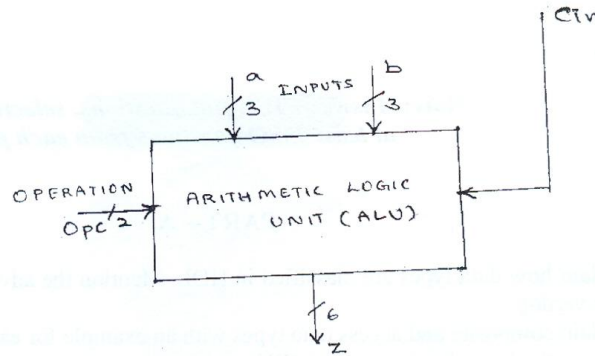


Fig.Q.6(b)

Assume the following operations: Addition, multiplication, division, no operation. (16 Marks)

- 7 a. How to invoke a verilog module from VHDL module? Explain with an example of a mixed language description for a full adder using two half adders. (10 Marks)
 b. Write a mixed language description of a 4-bit adder with zero flag. (10 Marks)
- 8 a. What is synthesis? List the general steps involved in synthesis. (08 Marks)
 b. Give synthesis information extracted, when the input and output are defined as:
 i) bit; ii) std-logic-vector. (04 Marks)
 c. Write a behavioural code in VHDL and verilog for the signal assignment statement $B = A$. Explain the mapping to gate level diagram. (08 Marks)

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06EC46

Fourth Semester B.E. Degree Examination, January 2013
Linear IC's and Applications

Time: 3 hrs.

Max. Marks:100

**Note: Answer FIVE full questions, selecting
at least TWO questions from each part.**

PART – A

- 1
 - a. Sketch an illustration to show the effect of op-amp slew rate and explain. State a typical op-amp slew rate. (05 Marks)
 - b. An op-amp inverting amplifier has a 0.5 volts input signal and its output is to be 9 volts. If feed back resistor $R_f = 12 \text{ K}\Omega$, calculate a suitable resistance value for R_i . (05 Marks)
 - c. Explain why the resistances at the two input terminals of an op-amp should be approximately equal in value. (04 Marks)
 - d. A non-inverting amplifier is to amplify a 100 mV signal to a level of 3 volts, using a 741 op-amp, design a suitable circuit. Assume bias current as 500 nA (max). (06 Marks)

- 2
 - a. How to set the upper cut-off frequency in an inverting amplifier circuit? Explain. (06 Marks)
 - b. Discuss the significance of using single polarity supply in an op-amp circuits. (06 Marks)
 - c. A capacitor-coupled voltage follower is to be designed to have a lower cut-off frequency of 120 Hz. The load resistance is $8.2 \text{ K}\Omega$ and the op-amp used has a maximum input bias current of 600 nA. Design a suitable circuit. (08 Marks)

- 3
 - a. Sketch the circuit of a lead compensation network. Explain its operation. Show how it affects operational amplifier frequency response. (08 Marks)
 - b. Write a note on Z_m mod compensation. (06 Marks)
 - c. A 741 op-amp with a slew rate of $0.5 \text{ V}/\mu\text{sec}$ is used as a voltage follower:
 - i) Calculate the slew rate limited cut-off frequency if the sine wave output is 5 volts.
 - ii) If this circuit is to operate with a unity gain cut-off frequency of 800 kHz, calculate the maximum peak value of the sinusoidal output voltage.
 - iii) If the upper cut-off frequency is 8 kHz, calculate the maximum value of the peak output voltage. (06 Marks)

- 4
 - a. Draw the circuit of a precision voltage source using an op-amp and a zener diode. Explain the circuit operation and derive the equation relating to V_o and V_z . (08 Marks)
 - b. Show the realization of current to voltage converter using an op-amp. (04 Marks)
 - c. Design an instrumentation amplifier to have an overall voltage gain of 900. The input signal amplitude is 20 mV; 741 op-amps are to be used and the supply is $\pm 15\text{V}$. (08 Marks)

PART – B

- 5
 - a. Show the realization of logarithmic amplifier using an op-amp. Obtain the expression for the output voltage. (08 Marks)
 - b. Sketch the circuit of a voltage follower type peak detector. Explain the circuit operation. (06 Marks)
 - c. Using 741 op-amp with a $\pm 9\text{V}$ supply design a phase shift oscillator to have an output frequency of 10 kHz. (06 Marks)

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- 6 a. Draw the circuits to show how diodes may be used to select the trigger points of an inverting Schmitt trigger circuit. Explain. (06 Marks)
- b. Sketch the circuit of a capacitor coupled zero-crossing detector. Show the waveforms at various points in the circuit and explain its operation. (08 Marks)
- c. Design a second order low pass filter to have a cut-off frequency of 1.5 kHz, using 741 op-amp. (06 Marks)
- 7 a. Define and explain the terms as applied to voltage regulator:
- i) Line regulation
 - ii) Load regulation
 - iii) Ripple rejection. (06 Marks)
- b. What is the principle of switch mode power supplies? Discuss the advantages and disadvantages. (08 Marks)
- c. Explain the operation of switching regulator using op-amp. (06 Marks)
- 8 a. With a neat block schematic, explain the operation of each component in PLL. (08 Marks)
- b. Write explanatory note on :
- i) 555 timer as monostable multivibrator
 - ii) A/D converters. (10 Marks)
- c. A PLL has free running frequency of 500 kHz and bandwidth of the low pass filter is 10 kHz. Will the loop acquire lock for an input signal of 600 kHz? Justify your answer. Assume that the phase detector produces sum and difference frequency components. (02 Marks)

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