CBCS SCHEME

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18EC61

Sixth Semester B.E. Degree Examination, June/July 2024
Digital Communication

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define Hilbert transform, list the properties and applications of Hilbert transform. **(06 Marks)**

b. Define pre-envelope of real valued signal. Given a band pass signal statement, sketch the amplitude spectra of signal statement, pre-envelope statement and complex envelope $\tilde{s}(t)$. **(06 Marks)**

c. Explain the time domain procedure for complex presentation of bandpass signals and system. **(08 Marks)**

OR

2 a. Obtain the canonical representation of band pass signals. **(07 Marks)**

b. What is line coding? For the binary stream 0110011 sketch the following line codes :
i) unipolar NRz
ii) polar MRz
iii) unipolar Rz
iv) bipolar Rz
v) Manchester. **(06 Marks)**

c. Derive the expression for complex low pass representation of band pass systems. **(07 Marks)**

Module-2

3 a. Explain the geometric representation of signals. Show that energy of signal is equal to the squared length of the vector representing it. **(07 Marks)**

b. Explain with a neat diagram and necessary equations the matched filter receiver. **(07 Marks)**

c. Explain the operation of correlation receiver with relevant diagrams. **(06 Marks)**

OR

4 a. Derive the expression for mean and variance of the correlator outputs. Also show that the correlator outputs are statistically independent. **(10 Marks)**

b. i) Using the Gram-Schemidt orthogonalization procedure, find a set of orthogonal basis functions to represent the three signals $S_1(t)$, $S_2(t)$ and $S_3(t)$ as shown in Fig.Q4(b)(i)
ii) Express each of these signals in terms of set of basis functions found on part(i).

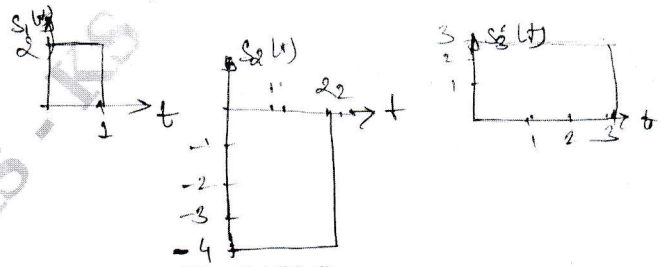

Fig.Q4(b)(i) **(10 Marks)**

Module-3

5 a. Explain BPSK system with the help of transmitter and receiver. Also derive the expression for probability of error of binary PSK. **(10 Marks)**

b. Explain with a neat block diagram generation and detection QPSK signals. **(06 Marks)**

c. Draw the signal-space diagram of M-ary QAM for M = 16. **(04 Marks)**

OR

6 a. Explain binary FSK. With a neat block diagram, describe a scheme for generating FSK signals. **(10 Marks)**

b. Explain with a neat diagram, generation and detection of DPSK signal. **(10 Marks)**

Module-4

7 a. What is ISI? Obtain the expression of output of a filter with inter-symbol interference. **(08 Marks)**

b. What are adaptive equilizers? Explain linear adaptive equalizer based on MSE criterion. **(08 Marks)**

c. Write a note on eye diagram. **(04 Marks)**

OR

8 a. Explain the design of band limited signals with controlled ISI. **(10 Marks)**

b. With a neat diagram, explain the concept of linear traversal filter. **(06 Marks)**

c. For the binary data sequence $\{d_n\}$ given as 111010010001101 determine the precoded sequence $\{i_n\}$, the transmitted sequence $\{a_n\}$, the received sequence $\{b_n\}$ and decoded sequence $\{d_n\}$. **(04 Marks)**

Module-5

9 a. Explain the generation and demodulation of DS spread spectrum signal. **(08 Marks)**

b. Explain with a neat block diagram, FH spread spectrum system. **(06 Marks)**

c. Mention the applications of DSSS and explain any one in detail. **(06 Marks)**

OR

10 a. With a neat diagram, explain the generation of PN sequence and state properties of ML sequences. **(08 Marks)**

b. Explain with a neat block diagram IS = 95 forward link. **(07 Marks)**

c. Explain the effect of dispreading on narrow band interference in DSSS system. **(05 Marks)**

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18EC62

Sixth Semester B.E. Degree Examination, June/July 2024
Embedded Systems

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the architecture of ARM Cortex-M3 processor with the help of a neat block diagram. **(07 Marks)**

b. List the application of ARM Cortex-M3 processor. **(07 Marks)**

c. Discuss the function of R_0 to R_{15} and other special registers in Cortex-M3 processor. **(06 Marks)**

OR

2 a. Explain ARM Cortex M3 program status registers in detail. **(08 Marks)**

b. Explain stack push and pop operation in Cortex-M3 with the help of a neat diagram. **(06 Marks)**

c. Explain and draw the organization memory map. **(06 Marks)**

Module-2

3 a. Explain the following instruction with an example:
(i) DMB (ii) RBIT (iii) UBFX (iv) BRC **(08 Marks)**

b. List and explain the function of any four data process and four branch instructions in ARM Cortex-M3 with an example. **(08 Marks)**

c. Write an ALP to find the sum of first 10 integer numbers. **(04 Marks)**

OR

4 a. Write a note on the CMSIS. **(08 Marks)**

b. Explain any two methods of accessing memory mapped registers (assembly code) in Cortex-M3. **(06 Marks)**

c. List and explain the function of any four commonly used memory access instructions in Cortex-M3 processor. **(06 Marks)**

Module-3

5 a. Explain the components of typical embedded system in detail. **(08 Marks)**

b. Write notes on the following:
(i) I2C (ii) IrDA (iii) Opto couple (iv) I - wire interface **(08 Marks)**

c. Differentiate between RISC and CISC architecture. **(04 Marks)**

OR

6 a. Explain the different on-board communication interface in brief. **(08 Marks)**

b. What are the different types of memories used in embedded system design? Explain role of each. **(08 Marks)**

c. Differentiate between Harvard and Von-Neumann architecture. **(04 Marks)**

Module-4

7 a. Explain the different characteristics of embedded system in detail. **(08 Marks)**

b. Explain the operational quality attributes of an embedded system. **(06 Marks)**

c. Explain the different embedded firmware design approaches in detail. **(06 Marks)**

OR

8 a. Explain the important non-operational attributes to be considered in any embedded system. **(08 Marks)**

b. What is Hardware and Software co-design? Explain the fundamental design approach in detail. **(08 Marks)**

c. Compare DFG and CDFG with an example and diagrams. **(04 Marks)**

Module-5

9 a. Briefly explain the function of the OS with a diagram. **(10 Marks)**

b. Write a block schematic of IDE environment for ESD and explain their function in brief. **(10 Marks)**

OR

10 a. Explain the terms process, task, threads. **(08 Marks)**

b. Explain briefly about simulator, emulator and debugging techniques. **(12 Marks)**

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18TE62

Sixth Semester B.E. Degree Examination, June/July 2024
Microwave Theory and Antennas

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

Module-1

1 a. With neat diagram, explain construction and operation of reflex klystron. **(10 Marks)**

b. A transmission line has the following parameters: R = 2Ω/m, G = 0.5mho/m, f = 1GHz, L = 8nH/m and C = 0.23pF. Calculate its characteristics impedance and propagation constant. **(05 Marks)**

c. Derive an expression for reflection coefficient when the transmission line is terminated by load impedance (Z_L). **(05 Marks)**

OR

2 a. Show the relationship between standing wave ratio and reflection coefficient. Also define reflection coefficient. **(08 Marks)**

b. A certain transmission line has characteristic impedance of 75 + j0.01Ω and is terminated in load impedance of 75 + j50Ω. Compute: i) Reflection coefficient ii) The transmission coefficient. **(06 Marks)**

c. What are high frequency limitations of conventional vacuum tube/transistors? **(06 Marks)**

Module-2

3 a. Explain S-matrix representation for multi-port network. **(06 Marks)**

b. In a H-Plane T-junction, computer power delivered to the loads 40ohms and 60ohms connected to arm 1 and 2 when 10MW power is delivered to matched port 3. Assume characteristic impedance of live = 50ohm. **(06 Marks)**

c. Define the following losses in microwave interms of S-parameters i) Transmission loss ii) Reflection loss iii) Return loss iv) Insertion loss. **(08 Marks)**

OR

4 a. Explain different types of co-axial connectors in microwave circuits. **(06 Marks)**

b. A magic T is terminated at collinear ports 1 and 2 and difference port 4 by impedances of reflection coefficients $r_1 = 0.5$, $r_2 = 0.6$ and $r_4 = 0.8$ respectively. If 1W power is fed at sum port 3, calculate the power reflected at port 3 and powder transmitted to other three ports. **(08 Marks)**

c. With a neat diagram, explain rotary precision phase shifter. **(06 Marks)**

Module-3

5 a. Show that the maximum effective aperture of short dipole is $0.119\lambda^2$. **(06 Marks)**

b. Discuss the different types of losses in microstrip lines. **(08 Marks)**

c. Calculate the exact directivity for 3-dimensional source having the pattern $U = U_m \sin^2\theta \sin^3\phi$ where $0 \le \theta \le \pi$, $0 \le \phi \le \pi$. **(06 Marks)**

OR

6 a. Explain the following parameters with respect to antenna:
i) Directivity ii) Beam area iii) Radiation intensity iv) Beam efficiency. **(08 Marks)**

b. Derive characteristic impedance of microstrip line with diagram. **(06 Marks)**

c. Compute the power received by receiving antenna kept at a distance of 100km by a transmitter radiating at 3MHz. Assume $G_T = 40$ and $G_R = 15$ and $P_T = 1000kW$. Derive relation used. **(06 Marks)**

Module-4

7 a. Derive an expression for radiation resistance of short electric dipole. **(10 Marks)**

b. Obtain the field pattern for two point sources situated symmetrically with respect to the origin. Two sources are feed with equal amplitude and equal phase signals. Assume distance between two sources = $\lambda/2$. **(10 Marks)**

OR

8 a. Obtain the expression for field of dipole in general for the case of thin linear antenna. **(10 Marks)**

b. Derive an array factor expression in case of linear array of 'n' isotropic point source of equal amplitude and spacing. **(10 Marks)**

Module-5

9 a. Discuss the following antenna types i) Helical antenna ii) Yogi-Uda antenna. **(10 Marks)**

b. Obtain the expression for radiation resistance of small loop antenna. **(10 Marks)**

OR

10 a. Explain helical geometry with diagram and practical consideration for mono-fillar axial mode helical antenna. **(10 Marks)**

b. Determine the length L_1 H-plane aperture and flare angle θ_E and θ_H of a pyramidal horn for which the E-plane aperture $\partial_E = 10\lambda$. The horn is fed by rectangular waveguide with TE_{10} mode. Let $\delta = 0.2\lambda$ in E-plane and 0.375λ, in H-Plane. Also find the beam widths and directivity. **(10 Marks)**

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18EC63

Sixth Semester B.E. Degree Examination, June/July 2024
Microwave and Antennas

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. With a neat diagram, explain construction and operation of reflex klystron. **(10 Marks)**

b. A line of $R_0 = 400\Omega$ is connected to a load of $200 + j300\Omega$ and is excited by a matched generator at 800MHz. Find the location and length of a single stub nearest to the load to produce an impedance match. **(10 Marks)**

OR

2 a. Derive transmission line equations in voltage and current forms. **(10 Marks)**

b. A telephone line has R = 6Ω/km L = 2.2mh/km C = 0.005μF/km and G = 0.05 μ mho/km. Determine z_0, α, β at 1 kHz. **(06 Marks)**

c. Define reflection coefficient and standing wave. **(04 Marks)**

Module-2

3 a. Explain the operation of a precision type variable attenuator with a neat sketch. **(10 Marks)**

b. Draw the diagram of magic tee and derive S-matrix of magic tee. **(10 Marks)**

OR

4 a. Draw the diagram of H-TEE and derive S-matrix for H-tee. **(08 Marks)**

b. A 20MN signal to fed into one of the collinear port 1 of a lossless H-plane T-junction. Calculate the power delivered through each port when other ports are terminated in matched load. **(04 Marks)**

c. For a two port network with mismatched load derive an expression for input reflection coefficient. **(08 Marks)**

Module-3

5 a. Define the following terms with respect to antenna:
- i) Beam area
- ii) Radiation intensity
- iii) Directivity
- iv) Beam efficiency
- v) Effective aperature. **(10 Marks)**

b. What are the losses in microstrip lines and briefly explain the same? **(10 Marks)**

OR

6 a. Obtain an expression for FRIS transmission formula used in radio communication link. **(08 Marks)**

b. A radio link has a 15W transmitter connected to an antenna of $2.5m^2$ effective aperature at 5GHz. The receiving antenna has an effective aperature of $0.5m^2$ and is located at a 15km line of sight distance from the transmitting antenna. Assuming lossless matched antennas find the power delivered to the receiver. **(06 Marks)**

c. A source has a radiation intensity pattern given by $U = U_m \sin\theta$. The radiation intensity 'U' has a value only in the upper hemisphere ($0 \leq \theta \leq x$) and ($\theta \leq \phi \leq 2x$). Find total power radiated by the source and directivity. **(06 Marks)**

Module-4

7 a. State and explain the power theorem. **(08 Marks)**

b. Derive an expression for total field in case of two isotropic point sources of same amplitude and phase. Plot the relative field pattern when these two isotropic sources are spaced $\lambda/2$ apart. **(12 Marks)**

OR

8 a. Derive an expression for total field for linear array of n isotropic point sources of equal amplitude and spacing. **(10 Marks)**

b. Derive the expression for the radiation resistance of short dipole. **(10 Marks)**

Module-5

9 a. Obtain the expression for radiation resistance of small loop antenna. **(10 Marks)**

b. With a neat diagram, explain the operation of log 'periodic antenna'. **(10 Marks)**

OR

10 a. Discuss the following antenna types:

i) Helical antenna

ii) Yagi uda antenna. **(10 Marks)**

b. Explain rectangular horn antenna with a neat diagram. **(10 Marks)**

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18TE63

Sixth Semester B.E. Degree Examination, June/July 2024
Computer Communication Network

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the three categories of connecting devices. **(10 Marks)**
b. Elaborate the OSI model in a layered frame work and explain. **(10 Marks)**

OR

2 a. Compare circuit switched network with packet switch network with diagrams. **(10 Marks)**
b. Explain the layer representation of the TCP/IP model. **(10 Marks)**

Module-2

3 a. With a neat diagram, explain ARP format. **(10 Marks)**
b. With an example, explain character stuffing and bit stuffing with neat diagram. **(10 Marks)**

OR

4 a. Describe 1-persistant, non-persistant and p-persistant methods of CSMA. **(10 Marks)**
b. Explain the layered model of the Bluetooth with a neat diagram. **(10 Marks)**

Module-3

5 a. Explain three phases of remote host and mobile host communication. **(10 Marks)**
b. Explain the operation of datagram approach with neat diagram. **(10 Marks)**

OR

6 a. Discuss IPv4 datagram format with diagram. **(10 Marks)**
b. With necessary example, explain the distance vector routing algorithm. **(10 Marks)**

Module-4

7 a. Explain three way Handshaking used in TCP protocol. **(10 Marks)**
b. Demonstrate stop and wait protocol with the help of ESMS and flow diagram. **(10 Marks)**

OR

8 a. Explain the TCP segment format with diagram. **(08 Marks)**
b. What are the services provided by UDP? Explain. **(06 Marks)**
c. Explain the domains of a network layer and a transport layer. **(06 Marks)**

Module-5

9 a. Explain the architecture of World Wide Web (WWW) with neat diagram. **(10 Marks)**
b. Write an algorithm for simple leaky bucket implementation, with neat diagram and explanation. **(10 Marks)**

OR

10 a. With a neat diagram, explain the FIFO queueing. **(10 Marks)**
b. Write the basic model of FTP and explain. **(10 Marks)**

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18EC644

Sixth Semester B.E. Degree Examination, June/July 2024
Digital System Design Using Verilog

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain logic level evolution in real-world circuits and define the term V_{OL}, V_{OH}, V_{IL} and V_{IH}. **(08 Marks)**

b. Explain simple methodology followed in IC industries with block diagram. **(08 Marks)**

c. Express the number $(4.5)_d$ in floating – point format with 5 bits of exponent and 12 bits of mantissa magnitude. **(04 Marks)**

OR

2 a. Develop a datapath to perform a multiplication of two complex numbers. The real and imaginary parts of the operands are represented as signed fixed-point numbers with 4 pre-binary-point and 12 post-binary-point bits. The real and imaginary parts of the products are similarly represented, but with 8 pre-binary-point and 24 post-binary points. **(08 Marks)**

b. Explain BCD code and 7-segment decoder and also write verilog model for that. **(08 Marks)**

c. Explain testbench and design under verification with proper diagram. **(04 Marks)**

Module-2

3 a. Explain basics of memory concept with proper symbol and calculate how many address lines and data lines are required for bellow memory size:
i) 64KB ii) 512MB **(08 Marks)**

b. Design 64K × 8 composite memory using 16K × 8 component. Note: Use common data input and output. **(08 Marks)**

c. List out difference between SRAM and DRAM. **(04 Marks)**

OR

4 a. Explain multi-port memory. List out advantages and disadvantages. Develop a verilog model of a dual-port. 4K × 16 – bit flow-through SSRAM. One port allows data to be written and read, while the other port only allows data to be read. **(08 Marks)**

b. Explain error detection and correction and also compute the 12-bit ECC word corresponding to the 8-bit data word 01010101. **(08 Marks)**

c. Explain pipelined SSRAM. **(04 Marks)**

Module-3

5 a. What is PLD? Explain the internal circuit of a PAL16L8 component. Specify the difference between PAL16L8 and PAL16R8. **(08 Marks)**

b. Explain output logic macrocell of a GAL22V10 component. Design priority encoder that has 08 inputs. The design is to be implemented in GAL22V10 component. **(08 Marks)**

c. Explain application specific integrated circuits. **(04 Marks)**

OR

6 a. Explain Xilinx Spartan-II FPGA logic block. **(08 Marks)**
b. Explain packaging and circuit boards. **(08 Marks)**
c. Explain differential signaling. **(04 Marks)**

Module-4

7 a. Explain the serial transmission of 64 bit data with suitable timing diagram. **(08 Marks)**
b. Explain Flash ADC and successive approximation ADC with diagram. **(08 Marks)**
c. Explain Firewire serial interface standards. **(04 Marks)**

OR

8 a. Explain polling and interrupts. **(08 Marks)**
b. Explain Gumnut I/O write and read operations with timing diagram. **(08 Marks)**
c. What are the purpose of control register and status register in I/O controller? **(04 Marks)**

Module-5

9 a. Explain prototypical design flow, including hardware/software co-design. **(10 Marks)**
b. What is design optimization? Explain optimization of area and power. **(10 Marks)**

OR

10 a. Explain Built-In-Self-Test (BIST) technique. **(10 Marks)**
b. Briefly explain following:
i) Fault models and fault simulation.
ii) Scan design and boundary scan. **(10 Marks)**

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