CBCS SCHEME

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BMATEC301/BBM301

Third Semester B.E./B.Tech. Degree Examination, June/July 2024
AV Mathematics – III for EC/BM Engineering

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. VTU Formula Hand Book and statistical table are permitted.
3. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Find the Fourier series for $f(x)=\begin{cases}-K, & \text{in } (-\pi,0)\\ K & \text{in } (0,\pi)\end{cases}$ and hence deduce $\frac{\pi}{4}=1-\frac{1}{3}+\frac{1}{5}-\frac{1}{7}+\ldots\ldots$	6	L2	CO1
	b.	Expand $f(x) = 2x - 1$ as a cosine half range Fourier series in $0 < x < 1$.	7	L2	CO1
	c.	Express y as a Fourier series upto the first harmonics given the following values: x: 0, 1, 2, 3, 4, 5 y: 4, 8, 15, 7, 6, 2	7	L3	CO1
		OR			
Q.2	a.	Find the Fourier series for $f(x) = x - x^2$ in $-1 < x < 1$.	6	L2	CO1
	b.	Show that half range sine series of $f(x) = \pi x - x^2$ in the interval $(0, \pi)$ is $\frac{8}{\pi}\sum_{n=0}^{\infty}\frac{1}{(2n+1)^3}\sin(2n+1)x$	7	L2	CO1
	c.	Obtain the Fourier series of y upto 2^{nd} harmonics f(x) is given by x: 0, $\pi/3$, $2\pi/3$, π, $4\pi/3$, $5\pi/3$, 2π f(x): 1.98, 1.30, 1.05, 1.30, -0.88, -0.25, 1.98	7	L3	CO1
		Module – 2			
Q.3	a.	Find the Fourier transform of $f(x)=\begin{cases}1-x^2, & \lvert x\rvert<1\\ 0 & \lvert x\rvert\ge 1\end{cases}$ and hence find the value of $\int_0^{\infty}\frac{x\cos x-\sin x}{x^3}dx$	6	L2	CO2
	b.	Find the Fourier sine and cosine transform of $f(x) = e^{-\alpha x}$, $\alpha > 0$.	7	L2	CO2
	c.	Solve the integral equation $\int_0^{\infty} f(\theta)\cos\alpha\theta\, d\theta=\begin{cases}1-\alpha, & 0\le\alpha\le 1\\ 0, & \alpha>1\end{cases}$ and hence evaluate $\int_0^{\infty}\frac{\sin^2 t}{t^2}dt$.	7	L3	CO2

		OR			
Q.4	a.	Find the Fourier transform of $e^{-a^2x^2}$, $a > 0$.	6	L2	CO2
	b.	Find the Fourier sine transform of $f(x) = e^{-\lvert x\rvert}$ and hence evaluate $\int_0^\infty \frac{x \sin mx}{1+x^2} dx$, $m > 0$	7	L2	CO2
	c.	Find the discrete Fourier transform of the sequence $\{1, 2, 1, 3\}^T$.	7	L3	CO2
		Module – 3			
Q.5	a.	Obtain the Z-transform i) $\cos n\theta$ ii) $\sin n\theta$.	6	L2	CO3
	b.	Find the inverse Z-transform of $\frac{3z^2+2z}{(5z-1)(5z+2)}$	7	L2	CO3
	c.	Solve by using Z-transforms : $y_{n+2} + 2y_{n+1} + y_n = n$ with $y_0 = 0 = y_1$.	7	L3	CO3
		OR			
Q.6	a.	Find the Z-transform of $2n + \sin\left(\frac{n\pi}{4}\right) + 1$	6	L2	CO3
	b.	Find the inverse Z-transform of $\frac{4z^2-2z}{(z-1)(z-2)^2}$.	7	L2	CO3
	c.	If $\bar{u}(z) = \frac{2z^2+3z+12}{(Z-1)^4}$ find the value of u_0, u_1, u_2.	7	L3	CO3
		Module – 4			
Q.7	a.	Solve $(D^4 + 8D^2 + 16)\, y = 0$.	6	L1	CO4
	b.	Solve $\frac{d^2y}{dt^2} - 4\frac{dy}{dt} + 13y = e^{3t} \cosh 2t$.	7	L2	CO4
	c.	Solve $x^3 + x^2y'' + xy' + 8y = 65 \cos(\log x)$.	7	L3	CO4
		OR			
Q.8	a.	Solve $y'' + 9y = \cos 2x \cos x$.	6	L2	CO4
	b.	Solve $(2x+1)^2 y'' - 2(2x+1)y' - 12y = 6x + 5$.	7	L2	CO4
	c.	In an LCR circuit, the charge q on a plate of a condenser is given by $L\frac{d^2q}{dt^2} + R\frac{dq}{dt} + \frac{q}{c} = E \sin pt$. Solve the equation for q.	7	L3	CO4

Module – 5

Q.9 **a.** Fit a straight line for the following data: (6, L1, CO5)

x	50	70	100	120
y	12	15	21	25

b. Obtain the lines of regression and hence find the coefficient of correlation for the data: (7, L2, CO5)

x	1	2	3	4	5	6	7
y	9	8	10	12	11	13	14

c. Compute the rank correlation coefficient for the following data: (7, L3, CO5)

x	68	63	75	50	62	80	78	40	55	60
y	62	58	68	45	81	60	68	48	50	70

OR

Q.10 **a.** An experiment on life time 't' of cutting tool at different cutting speeds v(units) are given below (6, L2, CO5)

Speed (v)	350	400	500	600
Life (t)	61	26	7	2.6

Fit a relation of the form $v = at^b$.

b. The following data gives the age of husband (x) and the age of wife (y) in years. Form the 2 regression lines and calculate the age of husband corresponding to 16 years of age of wife. (7, L2, CO5)

x	36	23	27	28	28	29	30	31	33	35
y	29	18	20	22	27	21	29	27	29	28

c. If the coefficient of correlation between the variables x and y is 0.5 and the acute angle between their lines of regression is $\tan^{-1}(3/5)$. Show that $\sigma_y = 2\sigma_x$. (7, L3, CO5)

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BEC302

Third Semester B.E./B.Tech. Degree Examination, June/July 2024
Digital System Design using Verilog

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	Define combinational logic. Give two examples.	4	L1	CO1
	b.	Explain the procedure to place a sum of products equation into canonical form. Express the function P = f(a, b, c) = ab′ + ac′ + bc in canonical form.	6	L2	CO1
	c.	Solve the function K = f(w, x, y, z) = Σ(0, 1, 4, 5, 9, 11, 13, 15) using Karnaugh map.	4	L2	CO1
	d.	Simplify the function F = f(P, Q, R, S) = Σm (0, 3, 5, 6, 7, 11, 14) using Quine-McCluskey method.	6	L2	CO1
		OR			
Q.2	a.	Define canonical sum of products and canonical product of sums. Give examples.	4	L1	CO1
	b.	Explain the procedure to place a product of sums equation into canonical form. Explain the function T = f(a, b, c) = (a + b′) (b′ + c) in canonical form.	6	L2	CO1
	c.	Solve the function G = f(a, b, c, d) = π(0, 4, 5, 7, 8, 9, 11, 12, 13, 15) using Karnaugh map.	4	L2	CO1
	d.	Simplify the function F = f(P, Q, R, S) = Σm(1, 2, 3, 5, 9, 10, 12) using Quine-McCluskey method.	6	L2	CO1
		Module – 2			
Q.3	a.	Define encoder. Write the truth table, equations and circuit diagram of 8 – to – 3 – line priority encoder.	4	L1	CO2
	b.	Explain the concept of carry-lookahead adder with related equations and block diagram.	6	L2	CO2
	c.	Design one-bit comparator with inputs A_i, B_i – bits to be compared, G_i, E_i, L_i – previous stage inputs and with the outputs G_{i+1}, E_{i+1}, L_{i+1}.	6	L4	CO2
	d.	Implement the function f(w, x, y, z) = Σm(0, 1, 5, 6, 7, 9, 12, 15) using 8 – to – 1 – line multiplexer.	4	L3	CO2

		OR			
Q.4	a.	Define decoder. Write the truth table, equations and circuit diagram of 3 – to – 8 – line decoder.	4	L1	CO2
	b.	Explain the operation of 8 – to – 1 line multiplexer with block diagram, truth table, equation.	6	L2	CO2
	c.	Construct parallel binary adder/subtractor using full adder block and EX-OR gates. Also explain the operation of it.	6	L3	CO2
	d.	Design two-bit comparator using cascade connection of one-bit comparators and explain its operation.	4	L4	CO2
		Module – 3			
Q.5	a.	State transparency property in latches. What is the need for master-slave flip flops?	4	L1	CO3
	b.	With neat block diagram and truth-table explain the operation of master-slave JK flipflop.	6	L2	CO3
	c.	Design a synchronous mod-6 counter using JK flipflops.	6	L4	CO3
	d.	Implement mod-4-ring counter using shift registers.	4	L3	CO3
		OR			
Q.6	a.	Define register and shift register. Mention two applications of shift registers.	4	L1	CO3
	b.	With logic diagram and timing diagram explain the operation of positive edge triggered D-flip flop.	6	L2	CO3
	c.	Design a four-bit binary ripple up-counter with logic diagram and counting sequence and briefly explain its operation.	6	L4	CO3
	d.	Implement Mod-8 twisted ring counter using shift registers and write the count sequence.	4	L3	CO3
		Module – 4			
Q.7	a.	List the different relational operators available in verilog language.	4	L1	CO4
	b.	Explain different verilog data types with examples.	6	L2	CO4
	c.	For the circuit diagram shown in Fig.Q.7(c), develop a verilog program for the output Y in: i) data flow description ii) behavioral description.	6	L3	CO4

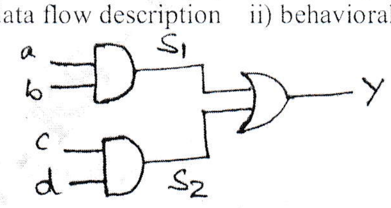

Fig.Q.7(c)

	d.	Develop a verilog program to implement 2 × 1 multiplexer using conditional operator. Also write the truth table of 2 × 1 multiplexer.	4	L4	CO4
		OR			
Q.8	a.	List the different styles of descriptions in verilog programming.	4	L1	CO4
	b.	Explain verilog shift operators and arithmetic shift operators with examples.	6	L2	CO4
	c.	Let A = 5'b11011, B = 5'b10101, C = 4'd3. Determine the output of the following verilog program statements: i) d = &A ii) e = ~^ 4'b1011 iii) f = ~(A & (~B)) iv) g = A || B v) b = 3 ** 2 vi) i = {2{A}}.	6	L3	CO4
	d.	Develop a verilog program for half subtractor using data flow description style by providing truth table and expressions.	4	L4	CO4
		Module – 5			
Q.9	a.	Write the verilog format of if-else statement and explain it.	4	L1	CO4
	b.	Explain the operation of positive triggered JK flipflop by writing verilog code using case statement and truth table.	6	L2	CO4
	c.	Develop a verilog behavioral description code for calculating the factorial of positive integers.	6	L3	CO4
	d.	Develop a verilog program for D-latch using behavioral description style by providing truth table.	4	L4	CO4
		OR			
Q.10	a.	Write the verilog format of case statement and explain it.	4	L1	CO4
	b.	Explain the operation of 2-to-1-line multiplexer by writing verilog structural description program and block diagram.	6	L2	CO4
	c.	Develop a verilog behavioral description code for three-bit binary up counter.	6	L3	CO4
	d.	Develop a verilog program for half adder using structural description style by providing truth table and expressions.	4	L4	CO4

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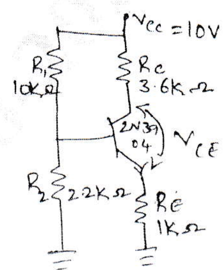
BEC303

Third Semester B.E./B.Tech. Degree Examination, June/July 2024

Electronic Principles and Circuits

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	With a neat circuit diagram, explain the voltage divider biasing circuit and also derive the expression.	10	L3	CO1
	b.	What is the collector-emitter voltage in Fig.Q1(b)  Fig.Q1(b)	10	L3	CO1
		OR			
Q.2	a.	With diagram explain the two transistors model. Also derive Z_{in}(base).	10	L3	CO1
	b.	Explain the base biased amplifier circuit. Also explain AC equivalent circuit.	10	L3	CO1
		Module – 2			
Q.3	a.	With diagram explain the enhancement model MOSFET. Draw Drain and Transconductance curve.	10	L3	CO2
	b.	Derive an expression of $i_D - V_{DS}$ relationship of NMOS transistor.	10	L3	CO2
		OR			
Q.4	a.	Derive an expression of DC bias point and voltage gain of small signal operation of MOSFET.	10	L3	CO2
	b.	With a neat diagram explain the MOSFET T-equivalent circuit.	10	L3	CO2
		Module – 3			
Q.5	a.	With diagram explain the R-2R ADC converter derive V_{out}.	10	L3	CO3
	b.	Derive V_{ref} and f_c of comparators with non zero reference to linear Amplifier.	10	L3	CO3
		OR			
Q.6	a.	With neat diagram explain the operational amplifier base wein bridge oscillator circuit.	10	L3	CO3
	b.	Explain the operation of RC phase shift oscillator.	10	L3	CO3
		Module – 4			
Q.7	a.	Briefly explain the four types of negative feedback.	10	L3	CO4
	b.	With diagram explain the ICVS amplifier circuit.	10	L3	CO4
		OR			
Q.8	a.	With diagram explain the passband and stopband attenuation.	10	L3	CO4
	b.	Explain with circuit diagram of VCVS High pass filter.	10	L3	CO4
		Module – 5			
Q.9	a.	With neat diagram explain the DC and AC two load line of VDB amplifier.	10	L3	CO5
	b.	Derive an expression of A_p of Class A power amplifier.	10	L3	CO5
		OR			
Q.10	a.	With circuit and waveform explain the 1-ϕ RC triggering circuit.	10	L3	CO5
	b.	With neat diagram explain the Triac – Diac based bidirectional phase	10	L3	CO5

CBCS SCHEME

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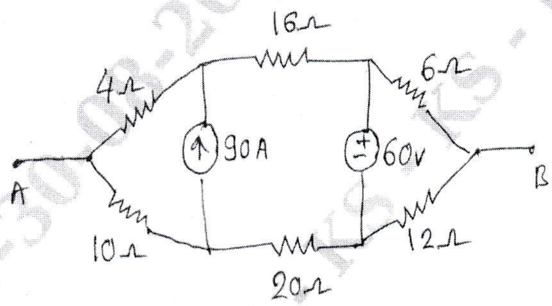
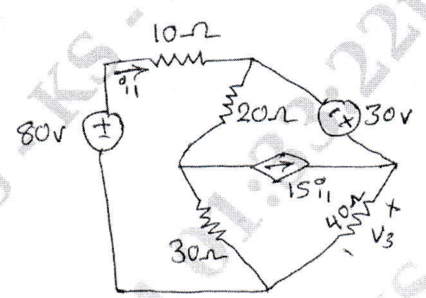
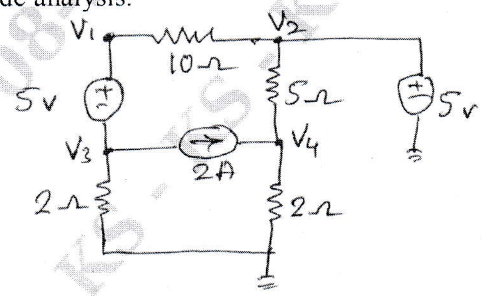
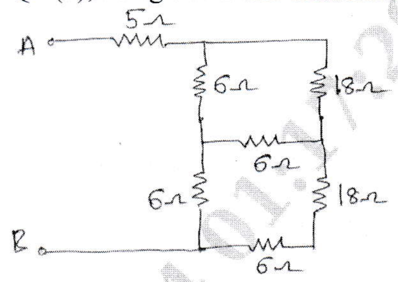
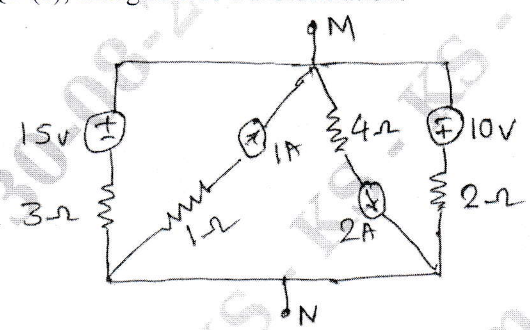
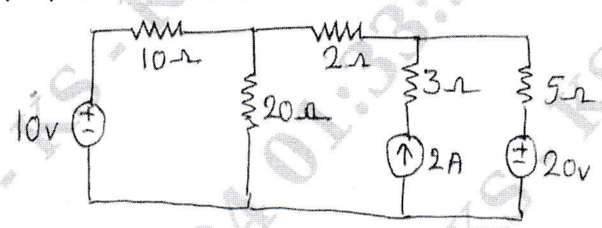
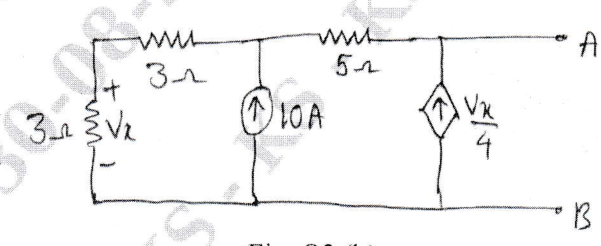
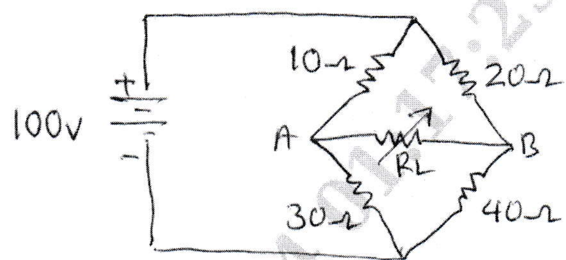
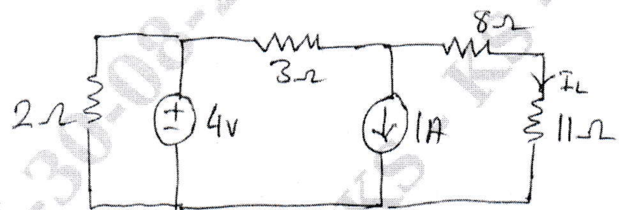
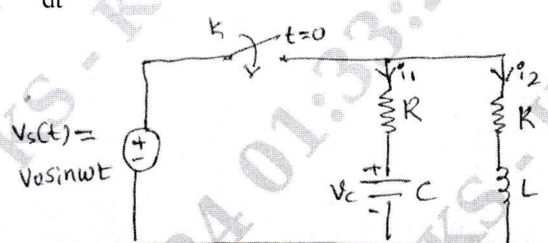
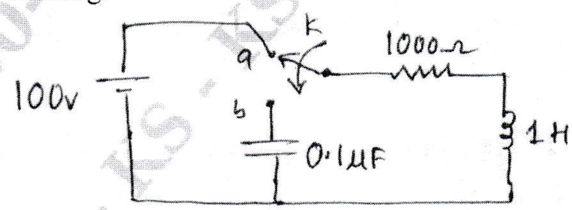
Third Semester B.E./B.Tech. Degree Examination, June/July 2024
Network Analysis

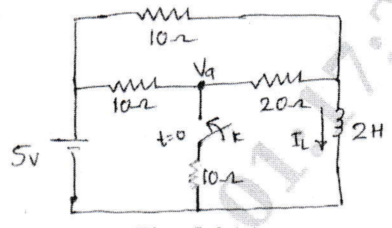
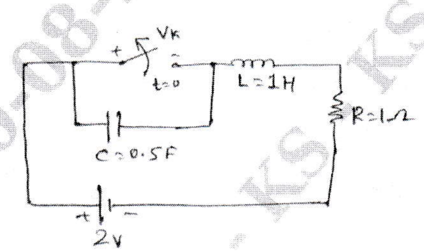
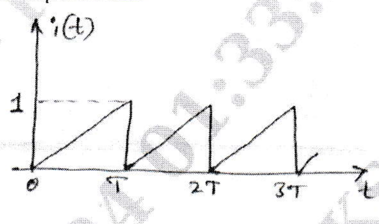
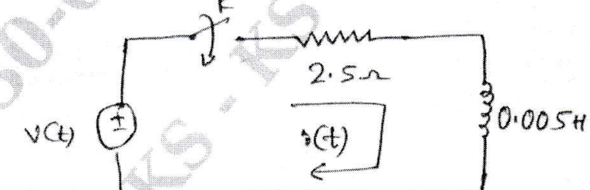
Time: 3 hrs. Max. Marks: 100

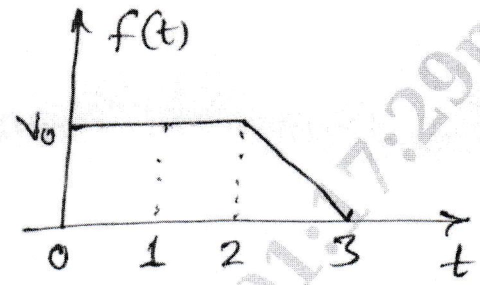
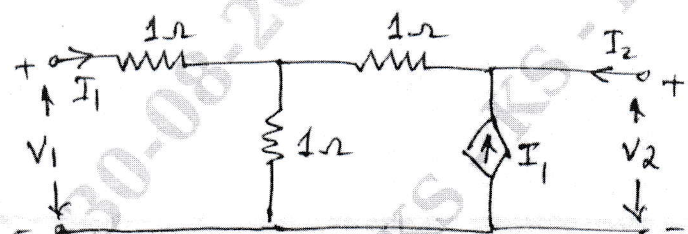
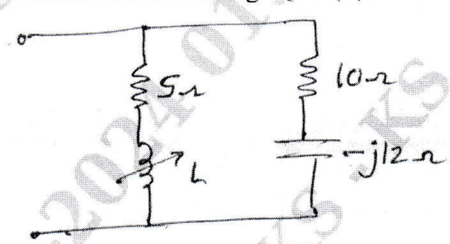
Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	**M**	**L**	**C**
Q.1	**a.**	Reduce the network shown in Fig. Q1 (a) to a single voltage source in series with resistance between terminals A and B. Use source transformation and source shifting technique.  Fig. Q1 (a)	**10**	**L3**	**CO1**
	b.	Determine voltage V_3 in the circuit shown in Fig. Q1 (b), using loop analysis.  Fig. Q1 (b)	**10**	**L3**	**CO1**
		OR			
Q.2	**a.**	For the network shown in Fig. Q2 (a), compute all node voltages V_1, V_2, V_3 and V_4 using Node analysis.  Fig. Q2 (a)	**8**	**L3**	**CO1**

	b.	Determine the equivalent resistance between terminal A and B, in the network shown in Fig. Q2 (b), using star Delta transformation.  Fig. Q2 (b)	7	L3	CO1
	c.	Find the potential difference between terminals M and N in the network shown in Fig. Q2 (c), using source transformation.  Fig. Q2 (c)	5	L3	CO1
		Module – 2			
Q.3	a.	Determine the voltage across 2Ω resistor in the circuit shown in Fig. Q3 (a), using the super position theorem.  Fig. Q3 (a)	10	L3	CO2
	b.	Find Thevenin's equivalent at terminal A and B, in the network shown in Fig. Q3 (b).  Fig. Q3 (b)	10	L3	CO2

		OR			
Q.4	**a.**	Determine the load resistance to receive maximum power from the source. Also find the maximum power delivered to the load in the circuit shown in Fig. Q4 (a).  Fig. Q4 (a)	8	L3	CO2
	b.	For the circuit shown in Fig. Q4 (b), determine current I_L using Norton's theorem.  Fig. Q4 (b)	8	L3	CO2
	c.	State Millman's theorem.	4	L2	CO2
		Module – 3			
Q.5	**a.**	In the network shown in Fig. Q5 (a), a switch K is closed at t = 0. Determine $\frac{di_1}{dt}, \frac{di_2}{dt}$ at $t = 0^+$.  Fig. Q5 (a)	10	L3	CO3
	b.	In the Network shown in Fig. Q5 (b), the switch K is changed position from a to b at t = 0. Solve for i, $\frac{di}{dt}, \frac{d^2i}{dt^2}$ at $t = 0^+$. The circuit is reached steady state before switching.  Fig. Q5 (b)	10	L3	CO3

		OR			
Q.6	**a.**	In the network shown in Fig. Q6 (a), steady state has been reached with switch K open. At time t = 0, the switch is closed. Deteremine the value of $V_a(0^-)$ and $V_a(0^+)$ at $t = 0^+$.  Fig. Q6 (a)	10	L3	CO3
	b.	In the network shown in Fig. Q6 (b), a steady state is reached with switch K closed. At t = 0, switch is opened. Determine voltage across switch V_K, $\frac{dV_K}{dt}$ at $t = 0^+$.  Fig. Q6 (b)	10	L3	CO3
		Module – 4			
Q.7	**a.**	State and prove initial and final value theorem in Laplace transformation.	10	L3	CO3
	b.	Obtain the Laplace transform of the waveform shown in Fig. Q7 (b). Assume that waveform is periodic.  Fig. Q7 (b)	10	L3	CO3
		OR			
Q.8	**a.**	In the series RL circuit shown in Fig. Q8 (a), the source voltage is $V(t) = 50 \sin 250t$ V. Using Laplace transform determine the current i(t) when switch K is closed at t = 0.  Fig. Q8 (a)	10	L3	CO3

	b.	Find Laplace transform of the waveform shown in Fig. Q8 (b).  Fig. Q8 (b)	10	L3	CO3
		Module – 5			
Q.9	a.	Find Z and ABCD parameters for the network shown in Fig. Q9 (a). Also verify whether network is Reciprocal or Symmetrical.  Fig. Q9 (a)	10	L3	CO4
	b.	A series RLC circuit has a resistance of 10 Ω, an inductance of 0.3 H and a capacitance of 100 μF. The applied voltage is 230 V. Find Resonance frequency, lower and upper cut-off frequencies, current at resonance, current at f_1 and f_2, voltage across inductance at resonance.	10	L3	CO4
		OR			
Q.10	a.	Derive Z-parameters in terms of H parameter.	8	L3	CO4
	b.	Find the value of L for which the circuit resonates at frequency of 1000 rad/sec, for the circuit shown in Fig. Q10 (b).  Fig. Q10 (b)	7	L3	CO4
	c.	Derive the relation between resonating frequency and half power frequencies i.e. $f_r = \sqrt{f_1 f_2}$	5	L2	CO4

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BEC306C

Third Semester B.E./B.Tech. Degree Examination, June/July 2024
Computer Organization and Architecture

Time: 3 hrs. Max. Marks: 100

Note: 1. Answer any FIVE full questions, choosing ONE full question from each module.
2. M : Marks , L: Bloom's level , C: Course outcomes.

		Module – 1	M	L	C
Q.1	a.	With a neat diagram, describe the functional units of a computer. Give examples for I/O.	10	L2	CO1
	b.	Write assembly language program for X = (A * B) + (C * D) using one address, two address, and three address instructions formats.	06	L3	CO1
	c.	Explain the Bus structures.	04	L2	CO1
		OR			
Q.2	a.	With a neat diagram, discuss the operational concepts in a computer highlighting the role of PC, MAR, MDR, IR.	10	L2	CO1
	b.	Discuss IEEE standard for single precision and double precision floating point numbers with standard notations.	06	L3	CO1
	c.	Distinguish between Big-endian and Little-endian memory assignment. With a neat sketch, show how the value 26789435 is stored using these methods.	04	L3	CO1
		Module – 2			
Q.3	a.	Define addressing mode. Explain any five addressing mode with syntax and examples.	10	L2	CO2
	b.	What is subroutine? With a pseudocode or program segment illustrate parameter passing using register.	05	L2	CO2
	c.	Explain various assembler directives used in assembly language program.	05	L2	CO2
		OR			
Q.4	a.	Explain stack operation with an example.	10	L2	CO2
	b.	Explain the shift and rotate operations with examples.	06	L2	CO2
	c.	Write a program to add 'n' number using indirect addressing mode.	04	L3	CO2
		Module – 3			
Q.5	a.	Showing the possible registers configuration in I/O interface. Explain program controlled input/output.	10	L2	CO3
	b.	Explain in detail the situations where a number of devices capable of initiating interrupts are connected to processor. How to resolve the problems?	10	L2	CO3
		OR			
Q.6	a.	What is an interrupt? With an example illustrate the concept of interrupt.	10	L2	CO3
	b.	Explain the Register involved in a DMA interface to illustrate DMA.	10	L2	CO3
		Module – 4			
Q.7	a.	Illustrate internal structure of static memory.	10	L2	CO4
	b.	With a neat diagram, explain virtual memory organization.	10	L2	CO4
		OR			
Q.8	a.	Classify memory in a computer. With a neat diagram, describe the organization of 2M × 8 DRAM chip.	10	L2	CO4
	b.	Briefly explain secondary storage devices.	06	L2	CO4
	c.	Explain use of a cache memory.	04	L2	CO4

Module – 5					
Q.9	**a.**	List different ways of improving CPU performance. With a neat diagram, discuss three-bus organization of CPU.	**10**	**L2**	**CO5**
	b.	Discuss Hardwired control unit organization with relevant diagrams and illustrate the logic to generate Z_{in} control signal.	**10**	**L3**	**CO5**
OR					
Q.10	**a.**	Explain single-bus organization of data path in a processor with neat diagram, highlight the importance of gating signals.	**10**	**L2**	**CO5**
	b.	Develop the complete control signal sequence for the instruction Add(R_1), R_3 with appropriate remarks.	**06**	**L3**	**CO5**
	c.	Discuss micro programmed control unit design with relevant diagrams.	**04**	**L2**	**CO5**

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