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15EC63

Sixth Semester B.E. Degree Examination, Jan./Feb. 2023
VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. With the help of diagrams, discuss various steps required to fabricate nMOS transistor. **(08 Marks)**

b. Discuss the working of nMOS transistor of enhancement type with the help of diagrams. **(08 Marks)**

OR

2 a. Explain the CMOS inverter DC characteristics highlighting the regions of operation. **(10 Marks)**

b. Explain the following non-ideal effects for short channel MOSFETs :
(i) Body effect
(ii) Channel length modulation **(06 Marks)**

Module-2

3 a. Construct stick diagram and layout for the expression $f = \overline{A(B+C)}$ using nMOS design style. **(10 Marks)**

b. Estimate nMOS inverter pair delay. **(06 Marks)**

OR

4 a. Derive an expression for rise time and fall time with respect to CMOS inverter. **(08 Marks)**

b. Construct layout for the expression $f = \overline{AB + CD}$ using CMOS design style. **(08 Marks)**

Module-3

5 a. Discuss different bus architectures. **(08 Marks)**

b. Discuss the design of 4 bit adder. **(08 Marks)**

OR

6 a. With relevant diagrams, discuss the operation of Manchester carry chain. **(08 Marks)**

b. Analyze the operation of 4 bit carry look-ahead adder using multiple output domino logic. **(08 Marks)**

Module-4

7 a. Discuss the operation of (n+1) lat parity generator with relevant circuit diagram and stick diagram. **(10 Marks)**

b. Discuss the design of data selectors. **(06 Marks)**

OR

8 a. Explain the architecture of field programmable gate array. **(10 Marks)**
b. Discuss the FPGA abstraction with diagram. **(06 Marks)**

Module-5

9 a. Explain three transistor DRAM with circuit diagram and stick diagram. **(08 Marks)**
b. Explain the operation of D-latch using nMOS and CMOS. **(08 Marks)**

OR

10 a. Illustrate the operation of scan based testing using serial scan technique. **(08 Marks)**
b. Explain the operation of Built In Logic Block Observation (BILBO) used in testing. **(08 Marks)**

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15EC64

Sixth Semester B.E. Degree Examination, Jan./Feb. 2023
Computer Communication Networks

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define data communication. What are the differences between half-duplex and full duplex transmission media? **(08 Marks)**

b. Identify five components of a data communication system and explain. **(08 Marks)**

OR

2 a. Explain TCP/IP protocol suite. **(08 Marks)**

b. What is framing? Explain bit-stuffing with an example. **(08 Marks)**

Module-2

3 a. Write the flow diagram of following random access protocols and explain:
(i) ALOHA
(ii) CSMA/CD
(iii) CSMA/CA **(09 Marks)**

b. A pure ALOHA network transmits 200 bits frames on a shared channel of 200 kbps. What is the throughput if the system (all station together) produces:
(i) 1000 frames per second
(ii) 500 frames per second
(iii) 250 frames per second **(07 Marks)**

OR

4 a. Define controlled access and explain the following controlled access methods:
(i) Reservation
(ii) Polling
(iii) Token passing **(08 Marks)**

b. What are the common Gigabit Ethernet implementations? Explain. **(08 Marks)**

Module-3

5 a. What are the differences between classfull addressing and classless addressing in IPV4? Explain the classfull addressing schemes. **(08 Marks)**

b. What is NAT? Explain how address translation is done in NAT. **(08 Marks)**

OR

6 a. Write the DHCP message format and explain working of DHCP. **(08 Marks)**

b. What is Bluetooth? Explain Bluetooth architecture and frame format. **(08 Marks)**

Module-4

7 a. Define fragmentation and explain fragmentation process. **(08 Marks)**

b. What is ICMP? Explain ICMP message format. **(08 Marks)**

OR

8 a. Explain the two internet debugging tools that use ICMP. **(08 Marks)**
b. With suitable diagram, explain distance vector routing. **(08 Marks)**

Module-5

9 a. What are the possible ambiguities in stop and wait ARQ protocol? **(03 Marks)**
b. With suitable flow diagram, explain what is the send window size and receive window size required for Go-Back-N protocol. **(07 Marks)**
c. Explain the concept of piggybacking technique. **(06 Marks)**

OR

10 a. With a neat diagram, explain briefly connection establishment, data transfer and connection termination in TCP. **(10 Marks)**
b. Give the comparison between TCP and UDP. **(06 Marks)**

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15EC651

Sixth Semester B.E. Degree Examination, Jan./Feb. 2023
Cellular Mobile Communication

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. What is Grade of Service? How are Erlang B formula and Erlang C formula used in cellular systems? **(08 Marks)**

b. A hexagonal cell within a four-cell system has a radius of 1.387km. A total of 60 channels are used within the entire system. If the load per user is 0.029 Erlangs and $\lambda = 1$ call/hour, compute the following for an Erlang C system that has a 5% probability of delayed call:
i) How many users per square km will this system support?
ii) What is the probability that a delayed call will have to wait for more than 10 seconds?
iii) What is the probability that a call will be delayed for more than 10 seconds?
Note: For 5% probability of delay with C = 15, traffic intensity = 9. **(08 Marks)**

OR

2 a. Mention and explain three basic propagation mechanisms used in a mobile communication system. **(06 Marks)**

b. Explain how Okumura model is used for signal prediction in urban areas. **(10 Marks)**

Module-2

3 a. Explain in detail the different factors influencing small scale fading. **(08 Marks)**

b. With the help of diagram, explain how spread spectrum sliding correlator technique used for small scale multipath measurements. **(08 Marks)**

OR

4 a. Classify and explain different types of small scale fading. **(08 Marks)**

b. Mean and median differ by 0.55dB in a Rayleigh fading channel. Justify. **(08 Marks)**

Module-3

5 a. With the help of diagram, explain GSM system architecture. **(08 Marks)**

b. With a simple block diagram, explain GSM speech coder. **(08 Marks)**

OR

6 a. Write and explain the classification of logical channels used in GSM. **(08 Marks)**

b. With the help of neat diagram, explain GPRS system architecture. **(08 Mark)**

Module-4

7 a. With the help of flow diagram, explain the process of location registration and location update. **(10 Marks)**

b. Explain the concept of
i) Intra cell and inter cell handover.
ii) Internal and External handover. **(06 Marks)**

OR

8 a. Summarize the concept of classical and popular GSM services provided in GSM system. **(08 Marks)**

b. Explain the effects of EDGE on the GSM system architecture. **(08 Marks)**

Module-5

9 a. Explain the network components found in CDMA 2000 wireless system. **(08 Marks)**

b. Draw the flow chart and explain the concept of CDMA mobile station initialization and call processing. **(08 Marks)**

OR

10 a. Explain the evolution of CDMA to 3G with a diagram. **(08 Marks)**

b. Explain different system activities involved in packet data service of CDMA 2000. **(08 Marks)**

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15EC663

Sixth Semester B.E. Degree Examination, Jan./Feb. 2023
Digital System Design using Verilog

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. What are the effects of capacitive loading and wire delay on signal transitions between logic levels? **(06 Marks)**

b. Explain hierarchical design methodology. **(05 Marks)**

c. Develop a verilog model for a 7-segment decoder. Include an additional input (blank) that overrides the BCD input and causes all the segments not to be lit. **(05 Marks)**

OR

2 a. Define the terms setup time, hold time and clock to output time of a flip flop. Explain the constraints imposed by these parameters on the circuit operations. **(06 Marks)**

b. Design a data path for a sequential complex multiplier whose operands and product are all in Cartesian form. The real and imaginary parts of the operands arc represented as signed fixed point numbers with 4 pre-binary point and 12 post binary point bits. Similarly, 8 pre binary point and 24 post binary point bits to be used for representing the product. Develop a verilog model for the same. **(10 Marks)**

Module-2

3 a. Design a 64K×8 bit composite memory using four 16K×8 bit components. Mention the advantages of using bidirectional tristate date connections in memory components. **(08 Marks)**

b. Explain the asynchronous static RAM with the timing diagram of read and write operations. **(08 Marks)**

OR

4 a. Describe multiport memories. Develop a verilog model of a dual port 4K×16 bit flow through SSRAM. One port allows data to be written and read, while the other port only allows data to be read. **(08 Marks)**

b. Determine whether there is an error in the ECC word 110111000110 and if so, correct it. **(05 Marks)**

c. Describe Flash memories. **(03 Marks)**

Module-3

5 a. Explain the internal organization of an FPGA. Also explain the internal structure of a Xilinx Spartan – II FPGA logic block with the diagram. **(08 Marks)**

b. Explain the signal integrity issues related with ASIC design. **(08 Marks)**

OR

6 a. Design a priority encoder to be implemented in a GAL22V10 component using the following specification. Priority encoder is to have 16 inputs I[0 : 15], a 4 bit encoded output Z[3 : 0] and a valid output that is 1 when any input is 1. Assume I[0] has the highest priority while I[15] has the lowest priority. **(05 Marks)**

b. How does differential signaling improves the noise immunity? **(05 Marks)**

c. What is PCB? Explain the different forms of PCBs. **(06 Marks)**

Module-4

7 a. With a neat diagram, explain the R-string DAC and R/2R ladder DAC. **(08 Marks)**

b. List and explain the different serial interface standards. **(08 Marks)**

OR

8 a. Illustrate an autonomous controller with an example. Also mention its advantages over simple controllers. **(08 Marks)**

b. Design an input controller that has 8 bit binary coded input from a sensor. The value can be read from an 8-bit input register. The controller should interrupt the embedded Gumnut core when the input value changes. The controller is the only interrupt source in the system. Develop a verilog model of this input controller. **(08 Marks)**

Module-5

9 a. Explain the design flow of Hardware/Software co-design. **(08 Marks)**

b. Explain the different power optimization techniques used in digital circuit design. **(08 Marks)**

OR

10 a. Explain the physical design in detail. **(08 Marks)**

b. Explain Built-In-Self-Test techniques. **(08 Marks)**

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