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15EC61

Sixth Semester B.E. Degree Examination, July/August 2022
Digital Communication

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define Hilbert Transform. What are its applications? List the properties and prove that a signal g(t) and its Hilbert Transform $\hat{g}(t)$ are orthogonal over the interval $(-\infty,+\infty)$. **(08 Marks)**

b. For a binary sequence 01000000001011, construct lines codes for the following: HDB3, B3ZS, B6ZS **(08 Marks)**

OR

2 a. Derive an expression for power spectral density of Bipolar NRZ format and plot the same with respect to frequency. **(08 Marks)**

b. Derive an expression for the complex low pass representation of bandpass system. **(08 Marks)**

Module-2

3 a. Explain Gram-Schmidt orthogonalization procedure. **(08 Marks)**

b. Derive an expression for maximum output SNR for matched filter receiver. **(08 Marks)**

OR

4 a. Explain the conceptual model of digital communication system with the aid of block diagram. **(08 Marks)**

b. Explain the geometric representation of signals. Show that energy of the signals is equal to the squared length of the vector representing it. **(08 Marks)**

Module-3

5 a. Derive an expression for probability of error for a BPSK modulated signal. **(08 Marks)**

b. Binary data are transmitted at a rate 10^6 Bps over a microwave link. Assuming channel noise is AWGN with zero mean and power spectral density at the receiver input is 10^{-19} watts/Hz. Compute the average carrier power required to maintain an average probability of error $P_e \leq 10^{-4}$ for coherent binary FSK. Compute the minimum channel bandwidth required. (Take u = 2.7 for erf(u) = 0.9998) **(08 Marks)**

OR

6 a. Describe the FSK signal with its signal space characterization, with relevant block diagram. Explain the generation and detection of FSK signal. **(08 Marks)**

b. A binary sequence 101101 is transmitted over a communication channel using DPSK transmitter. Assume the channel introduces a phase reversal of 180 degrees.

(i) Sketch the transmitted DPSK waveform assuming an initial bit of 1. What is the effect of changing the initial bit to 0?

(ii) Assuming the channel is noise free, show that the DPSK detector in the receiver produces the original binary sequence, deposit the 180 degrees phase reversal in the channel. For demonstration, take DPSK waveform with initial bit of 1. **(08 Marks)**

Module-4

7 a. Explain digital PAM transmission through band limited baseband channels with a neat block diagram. Obtain the expression for inter symbol interference. **(08 Marks)**

b. What is eye pattern? Explain with an example. Interpret the eye pattern for a baseband data transmission system, highlighting timing features. **(08 Marks)**

OR

8 a. Explain the operation of zero forcing linear equalizers with a relevant diagram and equations. **(08 Marks)**

b. Explain the raised cosine spectrum solution to reduce ISI with relevant graphs and expressions. **(08 Marks)**

Module-5

9 a. Explain the transmitter and receiver of frequency hop spread spectrum with necessary equations and block diagram. **(08 Marks)**

b. Illustrate the properties of maximum length sequences for an output sequences 0011101. **(08 Marks)**

OR

10 a. Explain the generation and demodulation of direct sequence spread spectrum signals with relevant equations and block diagram. **(08 Marks)**

b. Calculate Bit rate, PN sequence length. Bandwidth of PN sequence and processing gain of a DSSS system having the following parameters :
Bit duration = 4 ms
Chip duration = 2 μs **(08 Marks)**

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15EC63

Sixth Semester B.E. Degree Examination, July/August 2022
VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Derive an expression for I-V characteristics with neat diagram. **(10 Marks)**

b. Explain pseudo nMOS inverter and derive the dc characteristics graphically. **(06 Marks)**

OR

2 a. Explain the steps of n-well CMOS fabrication process with neat diagrams. **(10 Marks)**

b. Explain any two non-ideal IV effects in a MOSFET. **(06 Marks)**

Module-2

3 a. Illustrate the schematic, stick diagram and layout for the Boolean expression $Y = \overline{(A + BC)}$ (Implement using CMOS logic) **(10 Marks)**

b. Define standard unit of capacitance. Calculate the standard value of capacitance for MOS transistor in 5 μm, 2 μm and 1.2 μm technologies. Given gate capacitance for 5 μm = 4×10^{-4} pF/μm^2, gate capacitance for 2 μm = 8×10^{-4} pF/μm^2, gate capacitance for 1.2 μm = 16×10^{-4} pF/μm^2. **(06 Marks)**

OR

4 a. Derive an expression for the estimation of CMOS rise time delay and fall time delay. **(08 Marks)**

b. Explain the λ-based design rules for CMOS technology with neat diagrams. **(08 Marks)**

Module-3

5 a. Find the scaling factors for :
(i) Saturation current
(ii) Current density
(iii) Power dissipation/unit area
(iv) Maximum operating frequency. **(08 Marks)**

b. Describe Manchester carry-chain adder element. **(08 Marks)**

OR

6 a. Discuss the different bus architectures. **(08 Marks)**

b. With a neat diagram explain 4 × 4 Barrel shifter. **(08 Marks)**

Module-4

7 a. Realize NAND and NOR gate using Dynamic CMOS logic and explain its operation. **(08 Marks)**

b. Explain the 4-way data selector (multiplexer) with Boolean equation and nMOS based stick diagram. **(08 Marks)**

OR

8 a. Explain parity generator with the nMOS implementation of parity generator with stick diagram. **(08 Marks)**

b. Explain in detail the Generic Structure of FPGA architecture. **(08 Marks)**

Module-5

9 a. Explain 3-transistor dynamic RAM cell with neat diagram. **(08 Marks)**

b. Explain stuck at fault model in combinational circuits. **(08 Marks)**

OR

10 a. Demonstrate write operation and read operation for four transistor dynamic CMOS memory cell. **(08 Marks)**

b. Write a note on logic verification. **(08 Marks)**

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15EC64

Sixth Semester B.E. Degree Examination, July/August 2022
Computer Communication Networks

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. With layer diagram, explain the responsibility of each layer in OSI model. **(10 Marks)**

b. What different types of framing? Explain with a neat diagram the performance of a simplest protocol. **(06 Marks)**

OR

2 a. Discuss the performance of stop and wait ARQ protocol. **(06 Marks)**

b. Write short notes on Physical structures of networks. **(04 Marks)**

c. Compare and contrast OSI model with TCP/IP protocol suite. **(06 Marks)**

Module-2

3 a. With a flow diagram explain CSMA/CA protocol. **(04 Marks)**

b. Explain 1EEE802.3 MAC frame format. **(06 Marks)**

c. List the goals of fast Ethernet. Enumerate fast Ethernet implementation. **(06 Marks)**

OR

4 a. Explain any two method of controlled access of the channel. **(06 Marks)**

b. A pure ALOHA network transmits 200bit frames on a shared channel of 200kbps. What is the through put if the system (all stations together) produces?

i) 1000 frames per second

ii) 500 frames per second

iii) 250frames per second. **(06 Marks)**

c. What is the difference between unicast, multi cast and broad cast address Define the type of fallowing destination address.

4A : 30 : 10 : 21 : 10 : 1A

47 : 20 : 1B : 21 : 08 : EE

FF : FF : FF : FF : FF : FF **(04 Marks)**

Module-3

5 a. Explain with a neat diagram PCF implementation on top DCF in a infra structured network. **(06 Marks)**

b. Briefly explain 1EEE 802.11 addressing mechanism. **(06 Marks)**

c. Explain virtual LAN system and how the membership is allocated virtual LAN systems. **(04 Marks)**

OR

6 a. With a neat diagram, explain the specific functionalities of Bluetooth layers. **(06 Marks)**

b. Compare and contrast :

i) Classful and Classless addressing **(04 Marks)**

ii) Datagram and virtual circuit approach. **(06 Marks)**

Module-4

7 a. Discuss briefly the ICMP error reporting messages and also the ICMP debugging tools. **(08 Marks)**

b. Write short notes on :
i) Distance vector routing
ii) Link state routing. **(08 Marks)**

OR

8 a. Discuss briefly the three phases that the mobile host has to go through while communicating with remote host. **(08 Marks)**

b. Write short notes on :
i) Open shortest path first
ii) Border gateway protocol. **(08 Marks)**

Module-5

9 a. With a neat diagram, discuss :
i) User datagram format
ii) UDP services
iii) UDP applications. **(10 Marks)**

b. Discuss congestion control mechanism in TCP. **(06 Marks)**

OR

10 a. With a neat diagram, explain different fields of TCP segment. **(06 Marks)**

b. Write short notes on :
i) Flow control mechanism in TCP. **(06 Marks)**
ii) Error control mechanism in TCP. **(04 Marks)**

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15EC651

Sixth Semester B.E. Degree Examination, July/August 2022
Cellular Mobile Communication

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Explain all the Capacity Expansion Techniques, with a neat diagram. **(10 Marks)**
b. What are different Channel Assignment Strategies and explain the same. **(06 Marks)**

OR

2 a. Derive an expression for Free Space Propagation Model. **(06 Marks)**
b. Explain three basic propagation mechanisms. A total of 90 MHz of bandwidth is allocated to a FDD cellular telephone system which uses two 30KHz simplex channels to provide full duplex voice and control channels. Compute the number of channel available per cell if a system uses 4 cell reuse. **(10 Marks)**

Module-2

3 a. Explain the factors influencing the Small Scale Multipath propagation. **(08 Marks)**
b. Mention different types of Small Scale Fading and explain the same. **(08 Marks)**

OR

4 a. Explain Doppler shift. Consider a transmitter which radiates a sinusoidal carries frequency of 1850 MHz. For a vehicle moving 60 mph , compute the received carries frequency if the mobile is moving. i) Directly towards the transmitter ii) Directly away from the transmitter iii) In a direction which is perpendicular to the direction of arrival of the transmitter signal. **(10 Marks)**
b. With a neat diagram, explain Spread Spectrum Sliding Correlator Chanel Sounding. **(06 Marks)**

Module-3

5 a. Explain different GSM identities. **(08 Marks)**
b. Explain different burst in GSM system. **(08 Marks)**

OR

6 a. Explain the GSM Cellular Architecture , with neat diagram. **(08 Marks)**
b. Explain the GSM Signaling Model, with neat diagram. **(08 Marks)**

Module-4

7 a. Explain the Location update procedure in GSM system. **(10 Marks)**
b. Explain Mobile Initiated call termination in GSM network. **(06 Marks)**

OR

8 a. Explain the functioning of GPRS Network, with a neat diagram. **(08 Marks)**
b. Compare GPRS, HSCSO and EDGE techniques. **(08 Marks)**

Module-5

9 a. Explain the Channel concept in CDMA technology. **(10 Marks)**
b. Explain the Initialization and Registration procedure in CDMA technology. **(06 Marks)**

OR

10 a. Explain Mobile Originated call in CDMA technology. **(08 Marks)**
b. Explain the Reverse Logical concept in CDMA technology. **(08 Marks)**

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15EC663

Sixth Semester B.E. Degree Examination, July/August 2022
Digital System Design Using Verilog

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. What are the effects of Capacitive loading and propagation delay on signal transition between logic levels? **(08 Marks)**

b. Explain Simple design Methodology, with neat flow chart. **(08 Marks)**

OR

2 a. Write a note on Clocked Synchronous Timing Methodology. **(06 Marks)**

b. Develop a verilog model for 7 – segment decoder. Include an additional input blank, that overrides the BCD input and causes all segments not to be lit. **(06 Marks)**

c. What is the distinction between a Moore and a Mealy Finite – State machine? **(04 Marks)**

Module-2

3 a. Design a 64K × 8 bit composite memory using four 16K × 8 bit components and also explain bidirectional tristate data connection. **(08 Marks)**

b. Explain Asynchronous Static RAM. **(08 Marks)**

OR

4 a. Explain RD & WR Operations of DRAM. Also mention the common cause of soft errors in DRAM. **(06 Marks)**

b. Explain Multiport Memories. **(06 Marks)**

c. Determine whether there is an error in ECC word 000111000100 and if so correct it. **(04 Marks)**

Module-3

5 a. With a neat internal architecture, explain FPGA. **(08 Marks)**

b. Explain the concept of differential signaling. How does differential signaling improve noise immunity? **(08 Marks)**

OR

6 a. Explain the important measures to reduce the effect of ground bounce. **(06 Marks)**

b. Briefly explain EMI and Crosstalk. **(04 Marks)**

c. Explain Signal Integrity Interconnection issue in PCB design. **(06 Marks)**

Module-4

7 a. Explain any four Serial Interface Standard. **(08 Marks)**

b. Explain the mechanism for input/output controllers to request an interrupt. **(08 Marks)**

OR

8 a. Explain the Serial transmission of data and timing diagram for the serial receiver control. **(08 Marks)**

b. Explain the I/O bus protocol used by the Gumnut core. **(08 Marks)**

Module-5

9 a. Explain Fault models and Fault simulation. **(08 Marks)**

b. With a neat circuit diagram, explain 4 – bit LFSR and 4 – bit CFSR and their purposes. **(08 Marks)**

OR

10 a. Explain in brief design Optimisation for Area , Time and Power. **(08 Marks)**

b. Explain the Logical partitioning in Architecture Exploration with a neat block diagram of a Transport Monitoring System. **(08 Marks)**

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