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15EC61

Sixth Semester B.E. Degree Examination, Jan./Feb. 2021
Digital Communication

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. With neat diagram, explain Canonical representation of Band – pass signal. **(10 Marks)**

b. Obtain Hilbert transform of the following :

i) $x(t) = \cos 2\pi f_c t + \sin 2\pi f_c t$ ii) $x(t) = e^{-j2\pi f_c t}$ iii) $x(t) = \delta(t)$. **(06 Marks)**

OR

2 a. Explain the complex representation of band pass signals and systems. **(07 Marks)**

b. Given the data stream 1011100101. Sketch the pulses for each of the following line code :

i) Unipolar RZ ii) Bipolar NRZ iii) Manchester code

iv) Polar quarternary (Natural code). **(04 Marks)**

c. Write a short note on HDB3 signaling. **(05 Marks)**

Module-2

3 a. Using the Gram – Schmidt Orthogonalization procedure, find a set of Orthonormal basis functions to represent the three signals $S_1(t)$, $S_2(t)$ and $S_3(t)$, shown in Fig. Q3(a). **(10 Marks)**

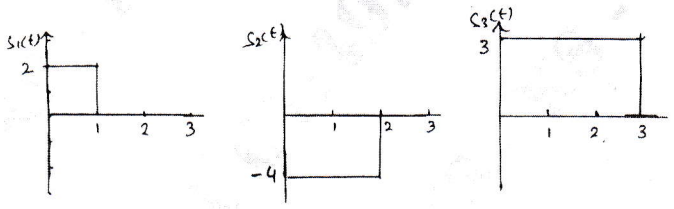

Fig. Q3(a)

b. Explain the matched filter receiver with mathematical expression. **(06 Marks)**

OR

4 a. Explain the Geometric representation of signals. Illustrate the geometric interpretation of signals for the case of 2 – dimensional signal space with 3 signals $S_1(3, 1)$, $S_2(1, 2)$, $S_3(2,3)$. **(07 Marks)**

b. Obtain the decision rule for ML decoding and explain Correlation receiver. **(09 Marks)**

Module-3

5 a. With a block diagram of QPSK transmitter and receiver, explain generation and demodulation of a QPSK wave. **(08 Marks)**

b. Obtain the expression for probability of error of BPSK. **(08 Marks)**

OR

6 a. With a neat diagram, explain the DPSK transmitter and receiver. **(07 Marks)**

b. Describe briefly M – ary QAM. Obtain the constellation of QAM for M = 4 and draw the signal space diagram. **(06 Marks)**

c. Draw the QPSK waveform for the sequence 0 1 1 0 1 0 0 0 showing in – phase and Quadrature components. **(03 Marks)**

Module-4

7 a. Explain the Nyquist criterion for distortion less base band binary transmission and obtain the ideal solution for zero ISI. **(08 Marks)**

b. What is Linear equalizer? With a neat diagram, explain the concept of equalization using a linear transversal filter. **(08 Marks)**

OR

8 a. With a neat block diagram, explain the digital PAM transmission through band limited base band channels and obtain the expression for ISI. **(06 Marks)**

b. What is Eye pattern? Explain with diagram, for binary and quaternary PAM and effect of ISI on eye opening. **(05 Marks)**

c. The binary sequence 1 1 1 0 1 0 0 1 0 0 0 1 1 0 1 is the input to the precoder. Obtain the precoded sequence, transmitted sequence , the received sequence and the decoded sequence. **(05 Marks)**

Module-5

9 a. With a neat block diagram, explain the concept of Frequency Hopped Spread Spectrum. **(07 Marks)**

b. Explain the effect of dispreading on a Narrow band interference with necessary diagram. **(04 Marks)**

c. Find the output sequence of the shift register shown in Fig. Q9(c). The initial state of the register is 1 1 1. Demonstrate the balance property and run property of a PN sequence. Also sketch the autocorrelation function. **(05 Marks)**

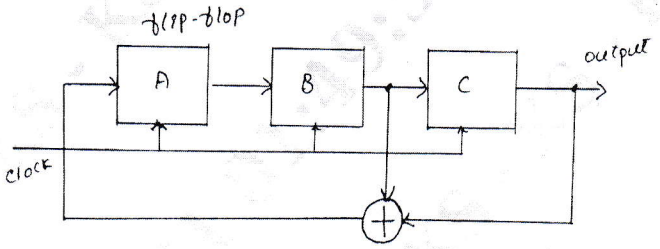

Fig. Q9(c)

OR

10 a. Explain the generation of Direct Sequence Spread Spectrum (DSSS) signal with relevant waveforms and spectrum. **(06 Marks)**

b. With a neat block diagram, explain the CDMA System based on IS – 95. **(07 Marks)**

c. Write a short note on Applications of Direct Sequence Spread Spectrum in CDMA. **(03 Marks)**

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15EC62

Sixth Semester B.E. Degree Examination, Jan./Feb. 2021
ARM Microcontroller and Embedded Systems

Time: 3 hrs. Max. Marks: 80

Note: *Answer FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Describe the functions of various units of the architecture of ARM Cortex M3 with neat block diagram. (07 Marks)

b. Explain 3 special function registers of ARM Cortex M3. (06 Marks)

c. State the applications of ARM Cortex M3. (03 Marks)

OR

2 a. Explain in detail the functions of registers $R_0 - R_{15}$ only of ARM Cortex M3. (04 Marks)

b. Explain in detail the operating modes of ARM Cortex M3 with switching diagrams. (06 Marks)

c. Describe the functions of exceptions with vector table ad priorities. (06 Marks)

Module-2

3 a. Explain Briefly about the basic syntax and the use of suffixes in assembly language instructions of Cortex M3 processor. (04 Marks)

b. Explain the following ARM Cortex M3 instructions with examples :
i) RSB ii) BIC iii) ASR iv) BFI v) SBFX vi) REVSH. (12 Marks)

OR

4 a. Construct and explain in detail the predefined memory map of Cortex M3. (12 Marks)

b. Write an ALP to find the sum of first 10 integer numbers 1 + 2 + 3 + - - - - + 10. (04 Marks)

Module-3

5 a. Compare embedded system and general purpose computing system. (04 Marks)

b. Explain the components of a typical embedded system in detail. (08 Marks)

c. Give the various application areas of embedded system. (04 Marks)

OR

6 a. Explain the different types of memories used in embedded system design. (05 Marks)

b. Explain in detail the SP2 communication interface with sequence of operation, for communicating with slave device. (05 Marks)

c. Explain the role of reset circuit and watch dog timer in embedded system. (06 Marks)

Module-4

7 a. Explain the characteristics of an embedded system. (05 Marks)

b. What is operational quality attribute? Explain the important operational quality attributes to be considered in any embedded system design. (08 Marks)

c. Explain the different communication buses used in automotive application. (03 Marks)

OR

8 a. With FSM model, explain the design and operation of automatic seat belt warning system. (05 Marks)

b. Explain the different firmware design approaches in detail. (08 Marks)

c. Bring out the advantages of high level language based firm ware development. (03 Marks)

Module-5

9 a. What is a kernel? Mention the functions of real time kernel. (04 Marks)

b. What is pre-emptive scheduling? Three processes with process ID's P1, P2, P3 with estimated completion time 10, 5, 7 ms and priorities 1, 3, 2 (0- highest priority, 3 – lowest priority) respectively enters the ready queue together. A new process P4 with estimated completion time 6ms and priority 0 enters the ready queue after 5ms of start of execution of P1. Calculate the average waiting time and turnaround time. (07 Marks)

c. Explain the transition of process with state transition diagram. (05 Marks)

OR

10 a. Explain out of circuit and in system programming methods for integration of firmware with hardware. (08 Marks)

b. Explain simulator based debugging and ICE based target debugging techniques. (08 Marks)

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15EC63

Sixth Semester B.E. Degree Examination, Jan./Feb. 2021
VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Explain the nmos enhancement mode transistor operation for different values of V_{GS} and V_{DS}. **(06 Marks)**

b. Obtain the transfer characteristics of a CMOS inverter mark all the region, showing the status of PMOS and nmos transistor. **(10 Marks)**

OR

2 a. Explain the fabrication steps of CMOS P-well process with neat diagram, and write all the mask sequence. **(10 Marks)**

b. Distinguish between CMOS and bipolar technologies **(06 Marks)**

Module-2

3 a. With neat diagram, describe the design rules i) Transistor ii) wires iii) contact cut. **(08 Marks)**

b. Draw the Schematic and Mask Layout for the expression $Y = \overline{AB + CD}$. **(08 Marks)**

OR

4 a. Derive the expression for the Rise time and fall time for CMOS inverter. **(10 Marks)**

b. Two MOS inverters are cascaded to drive a capacitive load C_L = 14cg as shown in Fig Q4(b). Calculate the pair delays V_{in} to V_{out} in terms of τ.

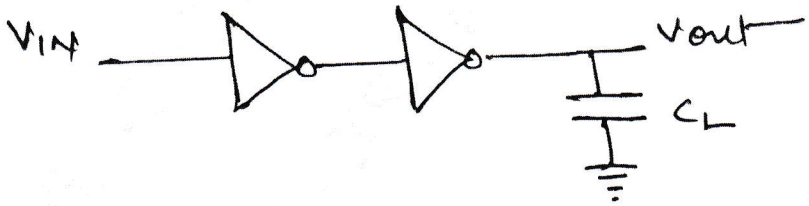

Fig Q4(b) **(06 Marks)**

Module-3

5 a. Why do we require scaling of MOS circuits? **(04 Marks)**

b. Find the scaling factors for the following :

i) Gate capacitance (C_g) ii) Saturation current (I_{ds})

iii) Gate capacitance per unit area (C_{ox}) iv) Carrier density in channel (Q_{ON})

v) Maximum frequency of operation (f_0) vi) Speed power product (P_T) **(12 Marks)**

OR

6 a. Discuss the General considerations of the subsystem Design process. (06 Marks)
b. Explain a standard Adder element using nmos version of adder logic. (10 Marks)

Module-4

7 a. Explain the multiplexer/Data selections with layout. (10 Marks)
b. Explain parity Generator with stick diagram. (06 Marks)

OR

8 a. Briefly explain Architecture of FPGA. (10 Marks)
b. Explain Antifuse base FPGA. (06 Marks)

Module-5

9 a. Explain one transistor DRAM. (08 Marks)
b. Explain Three Transistors DRAM. (08 Marks)

OR

10 a. Explain objectives of Functional Testing. (06 Marks)
b. Define fault model, explain the
i) Stuck – at Faults
ii) Stuck – open and stuck – short Fault
iii) Stuck – open Fault (10 Marks)

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15EC64

Sixth Semester B.E. Degree Examination, Jan./Feb. 2021
Computer Communication Networks

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the following briefly;
   i) Data flow
   ii) Star topology
   iii) LAN
   iv) WAN (08 Marks)

b. With a neat diagram, explain TCP/IP protocol suite along with relevant diagram. (08 Marks)

OR

2 a. With a neat diagram, explain link layer addressing in detail. (06 Marks)

b. Explain character oriented framing and Bit oriented framing. (05 Marks)

c. Explain stop and wait protocol with FSM diagram. (05 Marks)

Module-2

3 a. With a neat diagram, explain standard Ethernet frame format and addressing. (08 Marks)

b. Differentiate pure ALOHA and slotted ALOHA protocol. (04 Marks)

c. A slotted ALOHA network transmits 200 bit frames using a shared channel with a 200kbps bandwidth. Find the throughput if the system produces:
   i) 1000 frames per second
   ii) 500 frames per second
   iii) 250 frames per second. (04 Marks)

OR

4 a. With a neat flow diagram, explain CSMA/CD random access protocol along with different persistence methods. (08 Marks)

b. In the standard Ethernet with the transmission rate of 10Mbps, the length of the medium is 2500m and the size of the frame is 512 bits. The propogation speed of a signal in a cable is 2×10^8m/s. Calculate propogation delay, transmission delay and efficiency. (03 Marks)

c. What are the goals of fast Ethernet and explain Augonegotiation. (05 Marks)

Module-3

5 a. Explain two types of packet switched networks. (07 Marks)

b. Explain Hubs, link layer switches, routers. (06 Marks)

c. Differentiate basic service set and extended service set. (03 Marks)

OR

6 a. Explain classful addressing in detail. **(05 Marks)**

b. An organization is granted a block of addresses with beginning address 14.24.74.0/24. The organization needs to have 3 sub blocks of addresses to use in three subnets: one subblock of 10 addresses, one subblock of 60 addresses, and one subblock of 120 addresses. Design the subblocks. **(07 Marks)**

c. What is Bluetooth? Explain two types of Bluetooth networks. **(04 Marks)**

Module-4

7 a. Explain IPV4 Datagram format and header fields with diagrams. **(08 Marks)**

b. Explain distance vector routing along with distance vector routing algorithm for a node. **(08 Marks)**

OR

8 a. Explain ICMPV4 message formats with diagram and explain error reporting messages. **(08 Marks)**

b. What is path vector routing and explain the same? **(06 Marks)**

c. In an IPV4 packet, the value of HLEN is 5, and the value of the total length field is OX0028. How many bytes of data are being carried by this packet? **(02 Marks)**

Module-5

9 a. Explain connectionless and connection oriented protocols in transport layer. **(08 Marks)**

b. Explain Goback N protocol along with sliding window diagrams. **(08 Marks)**

OR

10 a. Explain TCP segment format along different fields. **(08 Marks)**

b. With a neat diagram, explain state transition diagram of TCP. **(08 Marks)**

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10EC63/10EC638

Sixth Semester B.E. Degree Examination, Jan./Feb. 2021

Microelectronics Circuits

Time: 3 hrs. Max. Marks:100

Note: Answer any FIVE full questions, selecting THREE questions from Part-A and TWO questions from Part-B.

PART – A

1 a. Explain the implementation of biasing circuit by fixing V_G and connecting a resistance in the source with neat diagram. **(06 Marks)**

b. Design the circuit in Fig.Q1(b) to establish a drain voltage of 0.1V. What is the effective resistance between drain and source at this operating point. Let V_t = 1V, $K_n'\left(\frac{W}{L}\right) = 1\ mA/V^2$.

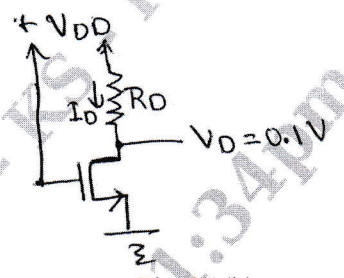

Fig.Q1(b) **(06 Marks)**

c. Explain common gate amplifier with neat circuit diagram and small signal equivalent circuit. **(08 Marks)**

2 a. Compare MOSFET and BJT in terms of :
(i) Low frequency hybrid π model
(ii) Current voltage characteristics
(iii) High frequency model **(06 Marks)**

b. With relevant equations and neat circuit diagram, explain working of MOS steering circuits. **(08 Marks)**

c. With neat diagram, explain working of basic MOS current mirror circuit. **(06 Marks)**

3 a. Draw high frequency equivalent circuit model of common source amplifier and analyze using Miller's theorem. **(08 Marks)**

b. Analyze common base amplifier to find R_{in} and R_{out}. **(07 Marks)**

c. How does cascade MOS current mirror improves the performance of current mirror circuit? **(05 Marks)**

4 a. With neat diagrams, explain small signal operation of MOS differential pair. Derive expression for differential gain. **(10 Marks)**

b. For circuit in Fig.Q4(b), the differential amplifier uses transistor with β = 100. Evaluate:
(i) Input differential Resistance R_{id}
(ii) Overall differential gain $\frac{V_0}{V_{sig}}$ (neglect effect of r_0)

(iii) The worst case common mode gain if the 2 collector resistances are accurate to within ±1%.
(iv) The CMRR in dB.
(v) The input common mode resistance (assume V_A = 100 V)

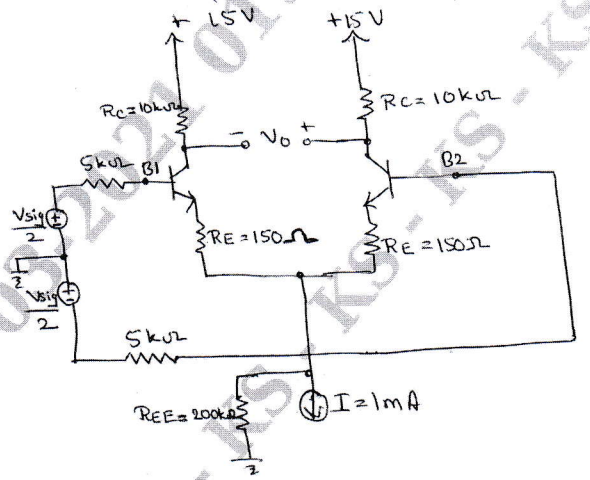

Fig.Q4(b) **(10 Marks)**

5 Write short notes on:
a. T-equivalent circuit model of MOSFET
b. Multistage amplifiers
c. Source follower
d. Current source **(20 Marks)**

PART – B

6 a. Explain the three properties of negative feedback. **(09 Marks)**
b. Draw and explain Nyquist plot of an unstable amplifier. **(05 Marks)**
c. With graph, explain how stability analysis is done using bode plot. **(06 Marks)**

7 a. With neat diagram, explain a single op amp difference amplifier and derive an expression for differential gain Ad. **(07 Marks)**
b. Briefly explain logarithmic amplifier and derive an expression for output voltage. **(08 Marks)**
c. Explain basic principle of sample and hold circuit using basic circuit. **(05 Marks)**

8 a. Write a short note on domino CMOS logic circuits. **(06 Marks)**
b. Implement $F = \overline{AB + \bar{A}\,\bar{B}}$ using AOI gate logic. **(08 Marks)**
c. Explain the Voltage Transfer Characteristics (VTC) of CMOS inverter when Q_N and Q_P are matched. **(06 Marks)**

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15EC651

Sixth Semester B.E. Degree Examination, Jan./Feb. 2021
Cellular Mobile Communication

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain capacity expansion techniques:
(i) Cell Splitting
(ii) Cell Sectoring
(iii) Micro zone concept **(08 Marks)**

b. For a mobile system of cluster size of 7, determine the frequency reuse distance if the cell radius is 5 km and also explain the concept of frequency reuse for cellular system. **(08 Marks)**

OR

2 a. With the help of equations, explain free space model. **(08 Marks)**

b. If a total of 33 MHz of bandwidth is allocated to a particular FDD cellular telephone system which uses two 25 kHz simplex channels to provide full duplex voice and control channels, compute the number of channels available per cell if a system uses:
(i) Four-cell reuse
(ii) Seven-cell reuse
(iii) Twelve-cell reuse **(08 Marks)**

Module-2

3 a. Explain the factors that influence small scale fading. **(06 Marks)**

b. Consider a transmitter which radiates a sinusoidal carrier frequency of 1850 MHz. For a vehicle moving 96.558 km/hr, compute the received carrier frequency if the mobile is moving towards the transmitter and away from transmitter. **(05 Marks)**

c. With neat block diagram, explain Direct RF pulse measurement, in small scale measurements. **(05 Marks)**

OR

4 a. Explain different types of small scale fading based on multipath time delay and Doppler spread. **(08 Marks)**

b. With relevant expressions, explain briefly Rayleigh and Ricean Distribution. **(08 Marks)**

Module-3

5 a. With the help of diagram, explain GSM architecture. **(08 Marks)**

b. With the help of diagram, explain basic elements of GSM transmission chain on the physical layer at the air interface. **(08 Marks)**

OR

6 a. What is Authentication and Encryption? Explain security related network functions in GSM. **(08 Marks)**

b. Explain protocol architecture of GSM signaling plane in detail. **(08 Marks)**

Module-4

7 a. Explain GPRS system architecture with interfaces with the help of neat diagram. **(08 Marks)**

b. Explain state model of a MS in GPRS. **(08 Marks)**

OR

8 a. Explain the logical channels used in GPRS. **(08 Marks)**

b. Explain Multimedia Messaging Service Network Architecture (MMSNA) with the help of neat diagram. **(08 Marks)**

Module-5

9 a. Explain different call hand offs in a CDMA system. **(08 Marks)**

b. With a block diagram, explain the generation of the CDMA paging channel. **(08 Marks)**

OR

10 a. Explain the IS-95 network architecture of a CDMA with neat diagram. **(08 Marks)**

b. With a block diagram, explain the generation of the CDMA forward traffic channel for 14.4 kbps traffic. **(08 Marks)**

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CBCS SCHEME

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15EC654

Sixth Semester B.E. Degree Examination, Jan./Feb.2021
Digital Switching System

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. With neat diagram, explain the hierarchy used in National Telecommunication Network. **(07 Marks)**

b. Explain the principles of operation of elementary TDM system with channel pulse trains. **(05 Marks)**

c. Express the following power levels in dBm and dBW:
(i) 1 mW (ii) 1 W (iii) 2 mW (iv) 100 mW **(04 Marks)**

OR

2 a. Draw a neat diagram of four-wire circuit and explain its working. **(07 Marks)**

b. Explain briefly the different network structures used in Telecommunication network. **(05 Marks)**

c. Write a short note on European Plesiochronous digital hierarchy. **(04 Marks)**

Module-2

3 a. Briefly explain message switching and circuit switching and also bring out the difference between them. **(07 Marks)**

b. What are the different functions of switching system? Explain briefly. **(05 Marks)**

c. Explain the cross bar system with matrix of cross points. **(04 Marks)**

OR

4 a. With the help of neat diagram, explain the Intra LM call and Inter LM call processing. **(08 Marks)**

b. With neat diagram, explain the function of Basic Central Office Linkages. **(05 Marks)**

c. Write a note on Electronic switching. **(03 Marks)**

Module-3

5 a. Derive the expression for Second Erlang's distribution starting from basic principles. **(07 Marks)**

b. Define grading. Explain different types of grading. **(04 Marks)**

c. In an average, during the busy hour, a company makes 180 outgoing calls of average duration of 3 minutes. It receives 400 incoming calls of average duration of 6 minutes. Find (i) the outgoing traffic (ii) Incoming traffic (iii) Total traffic. **(05 Marks)**

OR

6 a. Design a grading for connecting 20 trunks to switches having 10 outlets. **(06 Marks)**

b. Give the comparison between single stage and multistage networks. **(06 Marks)**

c. Define the following : (i) Holding time (ii) Congestion (iii) GOS (iv) Busy hour. **(04 Marks)**

Module-4

7 a. With neat diagram, explain the space switch. **(06 Marks)**

b. Briefly explain the Digital Switching System software classification. **(06 Marks)**

c. A T-S-T network has 20 incoming and 20 outgoing PCM highway, each conveys 30 channels, the required GOS is 0.01 and 0.02, find the traffic capacity of the network in mode-1 and mode-2. **(04 Marks)**

OR

8 a. With neat block diagram, explain S-T-S and T-S-T switching network. **(08 Marks)**

b. With the help of feature flow diagram, explain feature activation, feature operation and feature deactivation. **(08 Marks)**

Module-5

9 a. Draw neat block diagram and explain the organizational interfaces of typical DSS central office. **(08 Marks)**

b. Explain briefly with neat block diagram the generic switch hardware architecture. **(08 Marks)**

OR

10 a. Write a short note on software maintenance. **(04 Marks)**

b. Explain the common characteristics of Digital Switching System. **(06 Marks)**

c. Write the Analysis Report of digital switching system. **(06 Marks)**

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15EC663

Sixth Semester B.E. Degree Examination, Jan./Feb.2021
Digital System Design Using Verilog

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Construct with neat diagram, the simple design methodology and describe functions. **(08 Marks)**

b. Compute a design methodology for Hardware or Software codesign used in embedded system. **(08 Marks)**

OR

2 a. Construct and write verilog code for the Burglar alaram to be a priority Encoder, with zone 1 having highest priority, down to zone 8 having lowest priority, using truth table. **(08 Marks)**

b. Develop Data Path and Verilog model of the complex multiplier. **(08 Marks)**

Module-2

3 a. Design 64K*8 bit composite memory using four 16K*8 bit components. **(08 Marks)**

b. Describe all types of ROM. **(08 Marks)**

OR

4 a. Explain ECC code and and compute whether there is an error in the ECC word 000111000100, if so, correct it. **(08 Marks)**

b. Design and develop a verilog model of 7-segment decoder with blanking input using ROM. **(08 Marks)**

Module-3

5 a. With neat diagram, describe the Application Specific Integrated Circuits (ASICS). **(06 Marks)**

b. Compute design of Programmable Array Logic (PAL). **(10 Marks)**

OR

6 a. Compute the design of Field Programmable Gate Arrays (FPGA). **(10 Marks)**

b. Design a priority encoder has 16 inputs I[0:15]; four-bit encoded output Z[3:0]; & a valid output is 1, when any input I[0] has the highest priority and I[15]. The lowest priority. Express in verilog. **(06 Marks)**

Module-4

7 a. Describe all parallel buses used in digital circuits I/O devices. **(08 Marks)**

b. Describe all serial interface standard for connecting I/O devices. **(08 Marks)**

OR

8 a. Describe all types of interrupts used in I/O interfacing. **(08 Marks)**

b. Design an I/P controller that has 8-bit binary coded input from a sensor. The value can be read from an 8-bit input register. The controller should interrupt the embedded Gumnut core when the input value change. The controller is the only interrupt source in the system and design a verilog model of the input controller. **(08 Marks)**

Module-5

9 a. Describe area and time optimization used in design optimization. **(08 Marks)**

b. Describe scan design and boundary system. **(08 Marks)**

OR

10 a. Describe Built-In Self Test (BIST) using in Design methodology. **(08 Marks)**

b. Describe physical Design using in design flow. **(08 Marks)**

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