CBCS SCHEME

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15EC71

Seventh Semester B.E. Degree Examination, Aug./Sept. 2020
Microwaves and Antennas

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Explain the operation of Reflex Klystron with the help of neat sketch. **(06 Marks)**

b. A two-cavity Klystron operates at 5 GHz with a DC beam voltage of 10KV and 2mm cavity gap. For a given input RF voltage, the magnitude of the gap voltage is 100V. Calculate the transit time at the cavity gap, the transit angle, and velocity of the electrons leaving the gap. **(06 Marks)**

c. Define standing wave and standing wave ratio. **(04 Marks)**

OR

2 a. Derive transmission line equations. **(06 Marks)**

b. A certain transmission line has a characteristic impedance of 75 + j0.01Ω and is terminated in load impedance of 70 + j50Ω. Compute : i) reflection coefficient ii) transmission coefficient. **(06 Marks)**

c. Mention characteristics of Smith chart with the help of necessary equations. **(04 Marks)**

Module-2

3 a. Write short notes on :
i) Attenuator
ii) Phase shifters. **(08 Marks)**

b. Explain the properties of S-parameters for junction of ports having common characteristic impedance. **(08 Marks)**

OR

4 a. A 20 MW signal is fed into one of the collinear part 1 of a lossless H plane T junction. Calculate the power delivered through each port when other ports are terminated in matched load. **(04 Marks)**

b. Write the characteristics of Magic Tee. Also obtain scattering matrix for Magic Tee. **(08 Marks)**

c. Write short notes on : Coaxial connectors and adapters. **(04 Marks)**

Module-3

5 a. A microstrip line is composed of zero thickness copper conductors on a substrate having $\epsilon_r = 8.4$ $\tan\delta = 0.0005$ and thickness 2.4mm. If the line width is 1mm and operated at 10 GHz, calculate :
i) The characteristic impedance ii) the attenuation due to conductor loss and dielectric loss. **(08 Marks)**

b. Define the following :
i) Beam area
ii) Radiation resistance
iii) Beam efficiency
iv) Radiation intensity. **(08 Marks)**

OR

6 a. Obtain effective aperture and directivity of a half wave dipole. **(05 Marks)**

b. Derive Friis transmission formula. **(05 Marks)**

c. Obtain relationship between directivity and effective aperture. **(06 Marks)**

Module-4

7 a. Define power theorem. **(04 Marks)**

b. Find the directivity 'D' for the following sources with radiation intensity.
i) $U = U_m \sin^2\theta$, $0 \le \theta \le \pi$, $0 \le \phi \le 2\pi$ ii) $U = U_m \cos^2\theta$, $0 \le \theta \le \pi/2$, $0 \le \phi \le \pi/2$. **(05 Marks)**

c. Plot the field pattern for an array of two isotropic point sources with equal amplitude and same phase. Take $d = \lambda/2$. **(07 Marks)**

OR

8 a. Obtain the field pattern for a linear uniform array of isotropic antennas, satisfy the following $n = 5$, $d = \lambda/2$, $\delta = -d_r$. **(06 Marks)**

b. Derive an expression for radiation resistance of a short electric dipole. **(06 Marks)**

c. Explain principle of pattern multiplication with the help of suitable example. **(04 Marks)**

Module-5

9 a. Compare far fields of small loop and short electric dipole. **(04 Marks)**

b. Obtain an expression for radiation resistance of a loop antenna. **(06 Marks)**

c. Develop an expression for the field intensity ratio in the aperture plane for a parabolic reflector. **(06 Marks)**

OR

10 a. Determine the length L, H-plane aperture and flare angles θ_E and θ_H of a pyramidal horn for which the Eplane aperture $a_E = 10\lambda$. The horn is fed by a rectangular waveguide with TE_{10} mode. Let $\delta = 0.2\lambda$ in the Eplane and 0.375λ in the H plane. Also find the directivity. **(06 Marks)**

b. Define helix geometry. Explain practical design considerations for the monofilar axial mode helical antenna. **(06 Marks)**

c. Explain Yagi – Uda array with the help of diagram. **(04 Marks)**

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15EC73

Seventh Semester B.E. Degree Examination, Aug./Sept.2020
Power Electronics

Time: 3 hrs. Max. Marks: 80

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Give symbol , characteristic features of the following devices :
i) GTO ii) TRIAC iii) MOSFET. **(06 Marks)**

b. Explain different types of power electronic circuits with their input and output waveforms. **(06 Marks)**

c. Explain peripheral effects of power converter system. **(04 Marks)**

OR

2 a. Compare power MOSFET and bipolar junction transistor. **(04 Marks)**

b. Draw the switching model of MOSFET and explain its switching characteristics with neat figure. **(06 Marks)**

c. Explain output and transfer characteristics of IGBT. **(06 Marks)**

Module-2

3 a Explain the static anode – cathode characteristics of SCR. **(06 Marks)**

b. Explain the two transistor model of SCR and derive an expression for anode current in terms of current amplification factor and leakage current. **(06 Marks)**

c. The latching current of a thyristor circuit in fig.Q3(c) is 50mA. The duration of the firing pulse is 50μs. Will the thyristor get fired? **(04 Marks)**

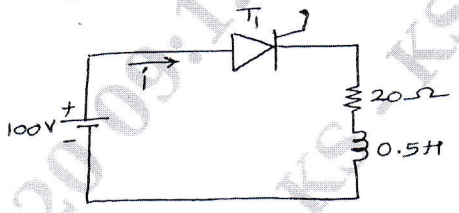

Fig. Q3(c)

OR

4 a. Distinguish between natural and forced commutation with examples. **(04 Marks)**

b. With a neat sketch, explain turn – off mechanism of SCR. **(06 Marks)**

c. With the help of neat circuit diagram and waveforms, explain the UJT firing circuit. **(06 Marks)**

Module-3

5 a. With a circuit diagram and waveforms, explain the working of a single phase full converter with a highly inductive load. Derive an expression for the average output voltage and rms output voltage. **(08 Marks)**

b. With a neat diagram and waveforms, explain the principle of single phase dual converter. **(06 Marks)**

c. Explain the role played by the free – wheeling diode in converters with R – L load. **(02 Marks)**

OR

6 a. Explain the principle of ON – OFF control, with the help of waveforms and derive an expression for rms output voltage. **(06 Marks)**

b. An AC voltage controller has a resistive load of R = 10 and the rms input voltage is 120V, 60Hz. The thyristor switch is ON for n = 25 cycles and is OFF for m = 75 cycles. Determine i) rms output voltage ii) the input power factor iii) the average and rms current of thyristor. **(04 Marks)**

c. Explain the operation of a single phase bidirectional controller with resistive load. Derive an expression for rms output voltage. **(06 Marks)**

Module-4

7 a. Explain the operation of step – down converter with RL load. Also derive an expression for peak – to – peak load ripple current. **(08 Marks)**

b. Explain with suitable circuit and waveforms, the principle of operation of step – up converter. Derive an expression for average output voltage of step-up converter. **(08 Marks)**

OR

8 a. Briefly explain the classification of the converter depending upon the directions of the current and voltage flows. **(05 Marks)**

b. With the help of circuit diagram and waveforms, explain the working of a Buck regulator. Derive the expression for peak – to – peak ripple current of the inductor. **(11 Marks)**

Module-5

9 a. Explain the operation of single phase half bridge inverter with R - load. Derive the expression for rms output voltage. **(08 Marks)**

b. Explain the performance parameters of inverters. **(08 Marks)**

OR

10 a. Explain the working of variable dc – link inverter. **(08 Marks)**

b. With a circuit diagram and waveforms, explain the working of a single phase full wave switch. Also derive an expression for average current and rms current of each thyristor. **(08 Marks)**

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15EC744

Seventh Semester B.E. Degree Examination, Aug./Sept.2020
Cryptography

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Find the greatest common divisor (1970, 1066) using Euclidean Algorithm and Explain the Algorithm. **(07 Marks)**

b. Explain Extended Euclid algorithm for (m, b). **(05 Marks)**

c. Define Rings and its axioms. **(04 Marks)**

OR

2 a. Define groups and fields. Explain its axioms. **(06 Marks)**

b. Explain polynomial Arithmetic, with an examples. **(05 Marks)**

c. List out the properties of modular Arithmetic for integers in Z_n. **(05 Marks)**

Module-2

3 a. With an example explain play fair cipher. **(09 Marks)**

b. Explain transposition techniques. **(04 Marks)**

c. What is Causal cipher? Give an example. **(03 Marks)**

OR

4 a. Encrypt a message "Paymole money" using a Hill cipher with the key

$$K = \begin{pmatrix} 17 & 17 & 5 \\ 21 & 18 & 21 \\ 2 & 2 & 19 \end{pmatrix}$$ **(08 Marks)**

b. With the help of block diagram explain single round of DES algorithm. **(08 Marks)**

Module-3

5 a. With the help of block diagram explain AFS Encryption and decryption. **(10 Marks)**

b. With a example explain 4-bit linear feedback shift registers. **(06 Marks)**

OR

6 a. Elaborate geffe generator, generalized geffe generator and stop-and-go generator of stream ciphers using LFSRs. **(08 Marks)**

b. With the help block diagram Beth-piper stop-and-go generator, alternating stop-and-go generator and Bilateral stop-and-go generator. **(08 Marks)**

Module-4

7 a. State and prove Felmat's theorem. **(05 Marks)**

b. Briefly explain RSA algorithm and key generation. **(07 Marks)**

c. Differentiate between conventional and public-key Encryption. **(04 Marks)**

OR

8 a. State and prove Euler's theorem. **(05 Marks)**

b. Discuss Diffie Hellman key exchange algorithm. Explain how the algorithm is used to exchange secret key. **(06 Marks)**

c. In RSA system it is given P = 17, q = 11, e = 7, M = 88. Find the cipher text C and message M from decryption. **(05 Marks)**

Module-5

9 a. Explain the requirements for message authentication codes. **(08 Marks)**

b. With the help of neat diagram, explain the message digital generation using SHA-512. **(08 Marks)**

OR

10 a. Explain direct digital signature and arbitrated digital signature. **(08 Marks)**

b. Explain MDS main loop. **(08 Marks)**

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15TE73

Seventh Semester B.E. Degree Examination, Aug./Sept.2020
CMOS VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. State and explain Moore's law. **(04 Marks)**

b. List the expressions for I_{ds} of an ideal MOS transistor for different regions of operation. **(03 Marks)**

c. Explain the CMOS inverter DC characteristics highlighting the regions of operation. **(09 Marks)**

OR

2 a. With the help of neat diagrams, explain the cutoff, linear and saturation region channel formation in nMOS transistor with different values of V_{gs} and V_{ds}. **(08 Marks)**

b. Briefly explain subthreshold condition and geometry dependence with respect to non-ideal I-V effects in MOS transistor with relevant expressions. **(08 Marks)**

Module-2

3 a. Draw the stick diagrams for :

(i) Simple n-well based BiCMOS inverter

(ii) Logic function $\overline{X} = A + B \cdot C$ in nMOS design style. **(08 Marks)**

b. Draw and explain in brief the design rules for wires in CMOS (λ based). **(08 Marks)**

OR

4 a. With the help of relevant figures and expressions, briefly explain the rise time and fall-time estimations with respect to CMOS inverter. **(08 Marks)**

b. With the help of a neat circuit diagram, explain the working of inverting type nMOS super buffer. **(08 Marks)**

Module-3

5 a. Draw the scaled nMOS transistor highlighting the scaling factors. **(06 Marks)**

b. Derive the scaling factors for the following device parameters:

(i) Gate Capacitance

(ii) Maximum Operating Frequency **(05 Marks)**

c. What are the problems associated with VLSI design? List the ways to reduce them. **(05 Marks)**

OR

6 a. Briefly explain the different Bus architectures with necessary figures. **(06 Marks)**

b. Implement the ALU functions line EX-OR, EX-NOR, AND and OR operations with an adder. Write the block diagram of 2-bit ALU using adder element. **(10 Marks)**

Module-4

7 a. With respect to gate restoration logic, draw the circuit diagram and stick diagram of 2-input NAND gate in nMOS and CMOS logic **(04 Marks)**

b. Briefly explain Pseudo-nMOS, Dynamic and Clocked CMOS logic. **(06 Marks)**

c. Design a parity generator and draw its nMOS stick diagram. **(06 Marks)**

OR

8 a. Explain the architecture of FPGA. **(08 Marks)**

b. With the help of a neat stick diagram, explain the working of 4:1 multiplexer. **(08 Marks)**

Module-5

9 a. Briefly explain the different fault models, observability and controllability with respect to manufacturing test principles. **(10 Marks)**

b. List out the System Timing considerations. **(06 Marks)**

OR

10 a. Explain the working of three transistor dynamic memory cell along with its circuit diagram and stick diagram. **(10 Marks)**

b. Briefly explain the Ad-hoc testing. **(06 Marks)**

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