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10EC/TE71

Seventh Semester B.E. Degree Examination, Aug./Sept. 2020

Computer Communication Networks

Time: 3 hrs. Max. Marks:100

Note: *1. Answer FIVE full questions, selecting atleast TWO questions from each part.*

2. Use of Handbooks /Charts/ Tables permitted.

PART – A

1 a. Discuss the responsibilities of the transport and physical layers with diagrams. **(08 Marks)**

b. With a neat diagram, explain the TCP/IP protocol suite in detail. **(07 Marks)**

c. Discuss the cable TV for data transfer. **(05 Marks)**

2 a. Explain the design, sliding window, window size of Go – Back – N ARQ protocol with relevant diagrams. **(10 Marks)**

b. In a stop – and – wait ARQ system, the band width of the line is 1 Mbps, 1 bit takes 20 ms to make a round trip.

i) What is the BW – delay product?

ii) What is the link utilization percentage if the number of frames are 1000?

iii) What is the link unitization percentage if the system can send 15 frames of 1000 bits long? **(03 Marks)**

c. Discuss the frame formats of three frames and explain the control field for S – frame. **(07 Marks)**

3 a. A pure ALOHA network transmit 200 bit frames on a shared channel of 200 Kbps. What is the throughput if the system produces?

i) 1000 frames/sec

ii) 500 frames/sec

iii) 250 frames/sec

Repeat the three cases for slotted ALOHA network. **(07 Marks)**

b. Explain the operation of CSMA/CD with its flow diagram, energy level, throughput. **(09 Marks)**

c. Explain the polling mechanism with its diagram. **(04 Marks)**

4 a. Discuss the goals and common implementations of fast Ethernet. **(07 Marks)**

b. Explain the frame format of 802.3 MAC frame. **(05 Marks)**

c. With a proper diagrams explain the hidden and exposed station problems and their effects. **(08 Marks)**

PART – B

5 a. Explain the following :

i) Bus back bone
ii) Star back bone
iii) Connecting remote LANs. **(06 Marks)**

b. What is a transparent bridge? Discuss the criteria to have a transparent bridge with relevant diagrams. **(10 Marks)**

c. Create a system of three LANs with four bridges. The bridges (B1 to B4) connect the LANs as follows :

i) B1 connects LAN1 and LAN 2
ii) B2 connects LAN1 and LAN 3
iii) B3 connects LAN2 and LAN3
iv) B4 connects LAN1, LAN2 and LAN3 choose B1 as the root bridge. Show the network, graph, spanning tree and blocking ports after applying spanning tree procedure. **(04 Marks)**

6 a. Discuss the datagram format of IPv4. **(07 Marks)**

b. Explain the transition strategies to move from IPv4 to IPv6. **(06 Marks)**

c. An ISP is granted a block of addresses starting with 150·80·0·0/16. The ISP needs to distribute these addresses to 3 groups of customers as follows :

i) The 1st group has 200 customers ; each needs 128 addresses
ii) The 2nd group has 400 customers ; each needs 16 addresses
iii) The 3rd group has 2000 customers ; each needs 04 addresses.

Design the sub blocks and find out how many addresses are still available after these allocations. **(07 Marks)**

7 a. Explain the types of routing table. Discuss the common fields in a routing table with its format. **(06 Marks)**

b. With relevant diagrams explain the concept of link state routing and 4 sets of actions to build a routing table. **(14 Marks)**

8 a. Explain the mechanism of client/server paradigm to achieve process-to-process communication. **(08 Marks)**

b. Discuss the name-address resolution. **(07 Marks)**

c. Discuss the data transfer of TCP connection. **(05 Marks)**

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10EC73

Seventh Semester B.E. Degree Examination, Aug./Sept.2020

Power Electronics

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. What is power electronics? Give two applications of power electronics. **(03 Marks)**

b. Explain the control characteristic of the following power devices:
(i) SCR (ii) TRIAC (iii) MCT (iv) SITH **(08 Marks)**

c. Explain briefly the different types of thyristor power converters and mention two applications of each. **(09 Marks)**

2 a. With necessary waveforms, explain the switching characteristics of a power transistor. **(08 Marks)**

b. Give the comparison between BJT, MOSFET and IGBT. **(06 Marks)**

c. The beta (β) of bipolar transistor is shown in Fig.Q2(c) below varies from 12 to 75. The load resistance $R_c = 1.5\Omega$. The dc supply voltage is $V_{CC} = 40$ V and input voltage to the base circuit $V_B = 6V$ if $V_{CE(sat)} = 1.2V$, $V_{BE(sat)} = 1.6V$, $R_B = 0.7\Omega$. Determine:
(i) Overdrive factor (ODF)
(ii) The forced beta
(iii) The power loss in the transistor P_T

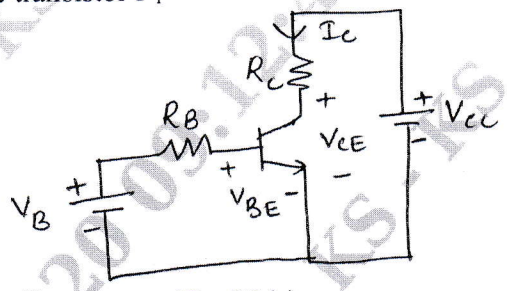

Fig.Q2(c) **(06 Marks)**

3 a. Explain the turn on mechanism of a thyristor using two transistor analogy and derive an expression for the anode current interms of transistor parameters. **(08 Marks)**

b. What is the need for protection of thyristors? Explain how thyristors are protected against high $\frac{di}{dt}$ and high $\frac{dv}{dt}$? **(06 Marks)**

c. With relevant circuit diagram and waveforms, explain the UJT firing circuit. **(06 Marks)**

4 a. With a neat diagram and waveform, explain the principle of single phase full converts with purely resistive load. Derive the expression for RMS output voltage and average output voltage. **(10 Marks)**

b. Compare circulating and non-circulating mode of operation of dual converter. **(04 Marks)**

c. How do you classify phase controlled converters? Explain. **(06 Marks)**

PART – B

5 a. Explain the operation of impulse commutation with the relevant circuit diagram and waveforms. **(08 Marks)**

b. In the circuit of Fig.Q5(b), the capacitor is initially charged to a voltage of $V_C(0) = 500$ V. If L = 15 μH and C = 50 μF and SCR is turned ON at t = 0. Calculate: (i) The peak value of resonant current (ii) The conduction type of thyristor

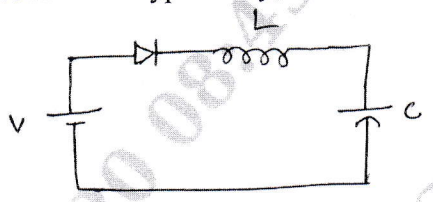

Fig.Q5(b) **(07 Marks)**

c. State the conditions under which a load carrying thyristor can be successfully commutated. **(05 Marks)**

6 a. Draw the circuit diagram of a single phase AC voltage controller and explain the principle of ON-OFF control, with the help of relevant waveforms. Derive the expression for RMS output voltage in terms of RMS supply voltage and duty cycle of the operation of the controller? **(10 Marks)**

b. An AC voltage controller in Fig.Q6(b) has a resistive load of R = 10Ω and the RMS input voltage is V_S = 120V, 60Hz. The thyristor switch is ON for n = 25 cycles and is off for m = 75 cycles. Determine:
(i) The output voltage, V_0
(ii) The input power factor (PF)
(iii) The average and RMS current of thyristors.

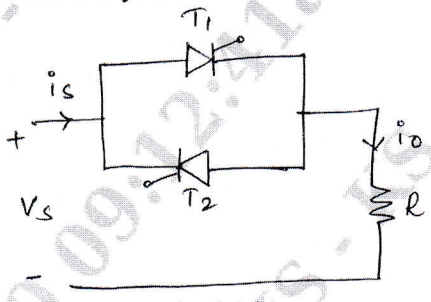

Fig.Q6(b) **(07 Marks)**

c. Distinguish between ON-OFF control and phase control. **(03 Marks)**

7 a. Explain the principle of operation of a step up chopper with suitable circuit diagram and waveforms. Derive the expression for average output voltage of step up chopper. **(10 Marks)**

b. Explain how choppers are classified. **(06 Marks)**

c. A DC chopper has an input voltage of 20V and a load of 8Ω resistance. The voltage drop across thyristor is 2V and the chopper frequency is 800 Hz. The duty cycle K = 0.4. Find:
(i) Average output voltage (ii) RMS output voltage (iii) Chopper efficiency **(04 Marks)**

8 a. Explain the performance parameters of inverters. **(06 Marks)**

b. A single phase full bridge inverter has a resistive load of 2.4 Ω and the DC input voltage 48V. Determine:
(i) RMS output voltage at the fundamental frequency
(ii) Output power. **(04 Marks)**

c. Explain the working of transistorized current source inverter. **(10 Marks)**

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10EC74

Seventh Semester B.E. Degree Examination, Aug./Sept.2020

Embedded System Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. What is an embedded system? What is the purpose of a watchdog timer in an embedded application? **(04 Marks)**

b. Briefly describe the major elements of embedded system development life cycle. **(08 Marks)**

c. Discuss the basic computing engines of an embedded system with suitable diagrams for each. **(08 Marks)**

2 a. What is meant by arity of an instruction? Explain the terms one, two, three address instruction. **(04 Marks)**

b. Briefly describe the more commonly used addressing modes. **(10 Marks)**

c. Describe these operations of instruction cycle in ISA and RTL level:
(i) Fetch (ii) Execute (iii) Next **(06 Marks)**

3 a. List and explain the various types of memory. **(06 Marks)**

b. Explain an associative mapping cache implementation. **(08 Marks)**

c. Explain the following: (i) Swapping (ii) Overlays **(06 Marks)**

4 a. What is a product life cycle and explain briefly V life cycle and spiral mode. **(08 Marks)**

b. Write a hardware architecture and data and counter flow diagram of a counter system and explain briefly flow diagrams. **(08 Marks)**

c. What are the five steps to a successful design? **(04 Marks)**

PART – B

5 a. What is scheduling strategy? Define the three general categories of scheduling strategy. **(06 Marks)**

b. Explain the core responsibilities of operating system. **(08 Marks)**

c. Define thread. Enumerate the difference between a process and thread. **(06 Marks)**

6 a. What is context switching? Explain with neat diagram. **(06 Marks)**

b. Write the algorithm for a simple OS Kernel, using C language notation for 3 asynchronous tasks using TCB's only. The 3 tasks use a common data buffer for read, increment and display operations. **(08 Marks)**

c. With a suitable schematic and program, explain the task control block. **(06 Marks)**

7 a. Explain the purpose of the complexity analysis by suggesting a suitable algorithm for that. **(08 Marks)**

b. Write short notes on Big O notation. **(05 Marks)**

c. Discuss the design of a memory map used in the memory loading, with an example. **(07 Marks)**

8 a. Define response time. Describe the major components of response time analysis of (i) polled loop (ii) pre-emptive scheduling, in an embedded application. **(08 Marks)**

b. With suitable algorithm, explain the analysis of search and sort to determine their complexity. **(08 Marks)**

c. What are the common mistakes that might be made during performance optimization analysis? **(04 Marks)**

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10EC751

Seventh Semester B.E. Degree Examination, Aug./Sept.2020

DSP Algorithms and Architectures

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the two methods of sampling rate conversions used in DSP system, with suitable block diagram and equations. **(06 Marks)**

b. List and explain the issues that have to be considered while designing and implementing a DSP system. **(04 Marks)**

c. The sequence x(n) = [0, 3, 6, 9] is interpolated using interpolation sequence b_K = [⅓, ⅔ , 1, ⅔,⅓] and the interpolation factor of 3. Find the interpolation sequence y(m). **(06 Marks)**

d. Discuss the advantages and disadvantages of FIR filter. **(04 Marks)**

2 a. Explain the circular addressing mode with the help of algorithm. **(06 Marks)**

b. What is the role of a shifter in DSP? Explain the implementation of 4-bit shift right barrel shifter with a diagram. **(08 Marks)**

c. Explain the different techniques used to prevent overflow and underflow conditions occurring in MAC unit. **(06 Marks)**

3 a. Draw the functional diagram of the barrel shifter of TMS320C54XX processor and explain its working. **(05 Marks)**

b. Assume that the current contents of AR3 is 400h, what will be its contents after each of the following TMS320C54XX addressing modes is used? Assume that the contents of AR0 are 40h. (i) *AR3+ (ii) *+AR3(–40h) (iii) *AR3+0 (iv) *AR3–0B **(04 Marks)**

c. With an example, explain memory mapped register addressing mode, absolute addressing mode and direct addressing mode. **(06 Marks)**

d. Explain the PMST register. **(05 Marks)**

4 a. Explain the function of various bits in Timer Control register. **(04 Marks)**

b. By means of a figure, explain the pipeline operation of the following sequence of TMS320C54XX instructions if the initial value of AR3 is 80 and the values stored in memory location 80, 81, 82 are 1, 2 and 3 respectively.

```
LD *AR3+, A
ADD *AR3+, A
STL A, *AR3+
```

(06 Marks)

c. Write an assembly language program of TMS320C54XX processor to compute the sum of three product terms given by the equation, $y(n) = h_0x(n) + h_1x(n-1) + h_2x(n-2)$ using MAC instructions. **(06 Marks)**

d. Describe the operation of the following instructions of TMS320C54XX processor:
(i) MPY *AR2–, *AR4+0, B
(ii) RPT # K **(04 Marks)**

PART – B

5 a. What values are represented by the 16-bit fixed point number N = 4000h in the Q_0, Q_7 and Q_{15} notations? **(06 Marks)**

b. Write an assembly language for TMS320C54XX processors to multiply two Q_{15} numbers to produce Q_{15} number result. **(06 Marks)**

c. Write a TMS320C54XX program that illustrates the implementation of an interpolating FIR filter of length 15 and interpolating factor 5. **(08 Marks)**

6 a. Briefly explain scaling and derive the expression for optimum scaling factor for DIT-FFT Butterfly algorithm. **(06 Marks)**

b. Write the subroutine for bit reverse address generation. Explain the same. **(08 Marks)**

c. Determine the following for a 512 point FFT computation:
   (i) Number of stages
   (ii) Number of butterflies in each stage.
   (iii) Number of butterflies needed for the entire computation. **(06 Marks)**

7 a. With a neat schematic diagram, design a data memory system with address range 000800-000FFFh for a C5416 processor. Use 2K × 8 SRAM memory chips. **(06 Marks)**

b. Draw the I/O interface timing diagram for read-write-read sequence of operation. **(04 Marks)**

c. Explain the ADC interface in programmed I/O mode. **(06 Marks)**

d. Explain the context registers required to configure DMA channels. **(04 Marks)**

8 a. With the help of block diagram, explain DSP-based biotelemetry receiver system. **(06 Marks)**

b. With the help of neat block diagram, explain PCM3002 CODEC. **(06 Marks)**

c. Explain JPEG encoding and decoding with the help of a block diagram. **(08 Marks)**

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15EC755

Seventh Semester B.E. Degree Examination, Aug./Sept. 2020
Satellite Communication

Time: 3 hrs. Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. State and explain Kepler's law of planetary motion. **(06 Marks)**

b. Explain phenomenon earth eclipse of satellite and fun transit outage. **(06 Marks)**

c. The apogee and perigee distances of a satellite orbiting in an elliptical orbit are respectively 45,000 km and 7000 km determine : i) semi major axis ii) orbit eccentricity iii) distance between the centre of the earth and centre of elliptical orbit. **(04 Marks)**

OR

2 a. Explain injection velocity and resulting satellite trajectories with supporting expressions. **(06 Marks)**

b. Explain ascending and descending nodes and equinoxes. **(06 Marks)**

c. Explain Azimuth angle and elevation angle. **(04 Marks)**

Module-2

3 a. Explain with neat schematic solar energy driven power system. **(06 Marks)**

b. Briefly explain fixed satellite earth station and mobile satellite service earth station. **(04 Marks)**

c. Explain with neat schematic tracking, delemetry and command subsystem. **(06 Marks)**

OR

4 a. Briefly explain altitude control and orbit control. **(04 Marks)**

b. Explain earth station architecture with generalized earth station block diagram. **(06 Marks)**

c. Explain monopulse tracking technique. **(06 Marks)**

Module-3

5 a. Explain MCPC systems with neat diagram. **(06 Marks)**

b. Derive expression for transmission equations. **(06 Marks)**

c. Write a short note on Free-space loss. **(04 Marks)**

OR

6 a. List advantages and disadvantages of TDMA over FDMA. **(04 Marks)**

b. With neat schematic explain DS – CDMA transmission and reception. **(06 Marks)**

c. Explain SDMA/FDMA system and SDMA/TDMA system with neat diagram. **(06 Marks)**

Module-4

7 a. Explain two types of transponders. (06 Marks)
b. Explain any six advantages of satellites over terrestrial networks. (04 Marks)
c. With neat diagram, explain satellite cable television. (06 Marks)

OR

8 a. Explain basic elements of a satellite communication system with neat sketch. (06 Marks)
b. Explain communication related applications of satellites. (04 Marks)
c. Write a short note on mobile satellite technology. (06 Marks)

Module-5

9 a. Explain in detail classification of satellite remote sensing systems. (06 Marks)
b. Write a short note on visible image and IR images. (06 Marks)
c. Explain in brief weather forecasting satellites orbits. (04 Marks)

OR

10 a. List and explain applications of remote sensing satellites. (08 Marks)
b. Explain working principle of GPS. (08 Marks)

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