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10EC/TE62

Sixth Semester B.E. Degree Examination, Aug./Sept.2020
Microprocessors

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Briefly explain the historical background of Intel microprocessors. **(04 Marks)**

b. With a neat block diagram, explain the BIU and EU of 8086 microprocessor. **(10 Marks)**

c. What is memory segmentation? List the advantages of memory segmentation. **(06 Marks)**

2 a. Write the instruction template for the following instructions. Also mention the encoded bits.

(i) MOV AX, BX (ii) MOV AL, [1234h]

(iii) MOV CL, [BX] [SI] (iv) MOV DX, 1568h **(08 Marks)**

b. What is the outcome of the following program segment:

(i)
```
MOV AL, 34h
MOV BL, 38h
SUB AL, BL
DAS
```

(ii)
```
MOV AL, 08h
MOV BL, 09h
MUL BL
AAM
```
(06 Marks)

c. What are assembler directives? Explain the following assembler directives:

(i) DW (ii) EQU (iii) PUBLIC (iv) EXTRN **(06 Marks)**

3 a. Write an ALP to generate factors of a given number. **(06 Marks)**

b. Explain string instructions, with an example for each. **(08 Marks)**

c. Distinguish between a MACRO and a PROCEDURE. Write an ALP that displays a carriage return and a line feed using a MACRO. **(06 Marks)**

4 a. Explain the software and hardware interrupt structure of 8086. **(10 Marks)**

b. Write a scheme to generate NMI interrupt on power failure and explain. **(10 Marks)**

PART – B

5 a. Interface a 4 × 4 keypad to 8086 CPU and write a program to identify a key pressed with relevant comments. **(12 Marks)**

b. Write an ALP to rotate stepper motor in clockwise direction of 180° and then in anticlockwise direction of 360°. **(08 Marks)**

6 a. Explain the data types of 8087 NDP. **(10 Marks)**

b. Represent 23.25 using long real (64 bit). **(04 Marks)**

c. Explain the following instructions of 8087 NDP with examples:

(i) FXCH (ii) FINIT (iii) FADD **(06 Marks)**

7 a. What are the different status and control signals generated on $\overline{s}_2$, $\overline{s}_1$ and $\overline{s}_0$ in maximum mode of 8086? Explain briefly. **(08 Marks)**

b. Write short notes on: (i) PCI (ii) USB (iii) LPT **(12 Marks)**

8 a. Briefly explain 80386 special registers. **(08 Marks)**

b. Write the salient features of 80486. **(06 Marks)**

c. Describe the basic features of Pentium processors. **(06 Marks)**

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10EC63

Sixth Semester B.E. Degree Examination, Aug./Sept. 2020
Microelectronics Circuits

Time: 3 hrs. Max. Marks:100

Note: *Answer any THREE full questions from Part-A and any TWO full questions from Part-B.*

PART – A

1 a. Derive an expression for drain current of a MOSFET in different regions of operation. **(05 Marks)**

b. Explain how the MOSFET can be used as an amplifier and as a switch. **(05 Marks)**

c. Explain different biasing methods in MOS amplifier circuits. **(10 Marks)**

2 a. Draw the development of the T-equivalent circuit model for the MOSFET. **(05 Marks)**

b. The NMOS and PMOS transistors in the circuit shown in Fig. Q2 (b) are matched with $K'_n\left(\frac{\omega_n}{L_n}\right) = K'_p\left(\frac{\omega_p}{L_p}\right) = 1\frac{mA}{V^2}$ and $V_{tn} = -V_{tp} = 1$ V. Assuming $\lambda = 0$ for both devices, find the drain currents i_{DN} and i_{DP} and the voltage V_0 for $V_I = 0$ V, +2.5V and – 2.5V . **(05 Marks)**

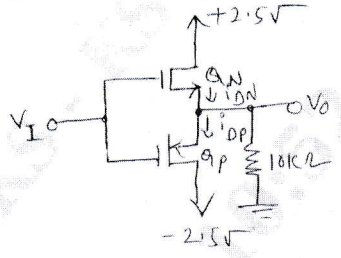

Fig. Q2 (b)

c. For a common gate amplifier with $g_m = 1$ mA/V and $R_D = 15$ KΩ. Find R_{in}, R_{out}, AV_O, A_V and G_V for $R_L = 15$ KΩ and $R_{sig} = 50$ Ω. What will the overall voltage can become for $R_{sig} = 1$ KΩ, 10 KΩ and 100 KΩ. **(10 Marks)**

3 a. What is MOSFET scaling? Explain about short channel effect due to scaling. **(05 Marks)**

b. Explain with neat diagram of Wilson MOS mirror. **(05 Marks)**

c. Given $V_{DD} = 3$V and $I_{REF} = 100$ μA it is required to design a basic MOSFET constant current source to obtain an output current whole nominal value is 100 μA. Find R if Q_1 and Q_2 are matched and have channel length's of 1 μm, channel width's of 10 μm, $V_t = 0.7$ V and $K'_n = 200$ μA/V^2. What is the lowest possible value of V_0? Assuming that for this process technology the early voltage $V'_A = 20$ V/μm, find the output resistance of the current source. Also, find the change in output current resulting from a+1-V change in V_0. **(05 Marks)**

d. Draw the BJT constant current source circuit and explain it. **(05 Marks)**

4 a. In common gate amplifier with active load, obtain 3-dB frequency for using open circuit time constants. Draw the circuit required for determining R_{gs} and R_{gd}. **(10 Marks)**

b. Consider a source follower circuit, specified as follows : W/L = 7.2 μm/0.36 μm, $I_D = 100$ μA, $g_m = 1.25$ mA/V, $\chi = 0.2$, $r_0 = 20$ KΩ, $R_{sig} = 20$ KΩ, $R_L = 10$ KΩ, $C_{gs} = 20$ fF, $C_{gd} = 5$ fF, $C_L = 15$ fF. Find three capacitances C_{gd}, C_{gs} and C_L. Find τ_H and the percentage contribution to it from each of three capacitances. Find f_H. **(10 Marks)**

5 a. Draw the two stage Op-Amp CMOS OpAmp configuration and briefly explain obtain overall open loop gain. **(08 Marks)**

b. The differential amplifier in figure uses transistors with $\beta = 100$. Evaluate the following:

(i) The input differential resistance R_{id}.

(ii) The overall differential voltage gain V_0/V_{sig} (Neglect the effect of r_0).

(iii) The worst case common mode gain if the two collector resistances are accurate to within $\pm 1\%$.

(iv) The CMRR in dB.

(v) The input common mode resistance (assuming that the early voltage $V_A = 100$ V) **(12 Marks)**

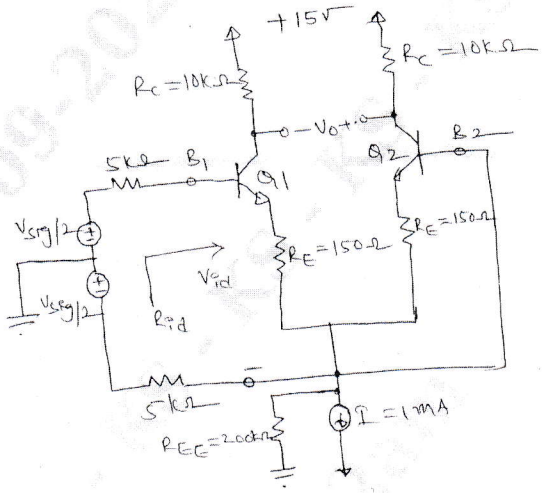

Fig. Q5 (b)

PART – B

6 a. Explain briefly with expressions the properties of Negative feedback. **(10 Marks)**

b. Explain about Shunt-Shunt feedback amplifier with diagram and obtain the expression for input impedance and output impedance. **(10 Marks)**

7 a. Explain instrumentation amplifier with neat circuit diagram. **(05 Marks)**

b. Use the superposition principle to find the output voltage of the circuit shown in Fig. Q7 (b). **(05 Marks)**

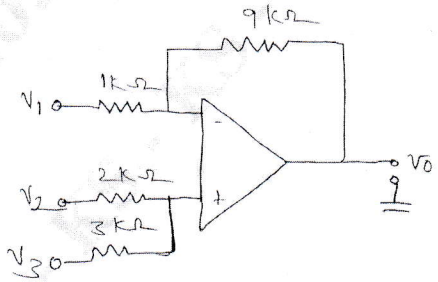

Fig. Q7 (b)

c. Explain logarithmic and antilogarithmic amplifiers with neat diagrams. **(10 Marks)**

8 a. Explain the dynamic operation of a CMOS inverter. **(10 Marks)**

b. Sketch a CMOS logic circuit that realizes the function $Y = \overline{ABC + DE}$, using AOI gate. **(04 Marks)**

c. Explain charge sharing problem in dynamic 3-input NAND circuits. **(06 Marks)**

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10EC64

Sixth Semester B.E. Degree Examination, Aug./Sept.2020
Antennas and Propagation

Time: 3 hrs. Max. Marks:100

Note: *Answer any FIVE full questions, selecting atleast TWO questions from each part.*

PART - A

1 a. Explain the following terms with respect to an antenna :
i) Radiation intensity ii) Beam area iii) Polarization. **(06 Marks)**

b. Deduce the expression to depict the relation between effective aperture and directivity. **(07 Marks)**

c. Derive the expression for a field at a particular point in free space. **(07 Marks)**

2 a. Determine the actual directivity and approximate directivity for : i) $U = U_m \cos^3 \theta$
ii) $U = U_m \sin\theta \sin^2\phi$ iii) $U = U_m \sin\theta \sin^3\phi$ for $0 \le \theta, \phi \le \pi$. **(10 Marks)**

b. A linear array of 4 point sources has a distance of N_2 between adjacent elements of the array. The power is applied with equal amplitude and a phase difference of $-d_r$. Obtain the field pattern. **(10 Marks)**

3 a. Deduce the expression for the electric field component of a linear antenna of length N_2. **(12 Marks)**

b. Illustrate that the radiation resistance of a short dipole is 73Ω. **(08 Marks)**

4 a. Derive the expression for electric field component of a small circular loop antenna of radius 'a' carrying current I. **(08 Marks)**

b. State and illustrate Babinets principle. **(06 Marks)**

c. Deduce the expression for radiation resistance of a loop antenna. **(06 Marks)**

PART - B

5 a. Explain the Slot antenna and Complementary antenna. **(06 Marks)**

b. Explain the features and operation of helical antenna with its modes of operation. **(07 Marks)**

c. Explain the working of Yagi – Uda antenna. Mention its applications. **(07 Marks)**

6 a. Explain Rumsey's principle and the operation of log periodic antenna. **(10 Marks)**

b. Describe the operation of i) Antennas for ground penetrating radar ii) Embedded antenna. **(10 Marks)**

7 a. Deduce the resultant field strength due to direct and ground related rays at a distance 'd' from the transmitter , 'h_t' is the height of the transmitter and 'h_r' is the height of the receiver. **(10 Marks)**

b. Describe the factors affecting ground wave propagation. **(06 Marks)**

c. A VHF communication is to be established at 90MHz, with the transmitter power of 35W. Calculate the LOS communication distance, if the height of transmitter and receiver antenna are 40m and 25m respectively. **(04 Marks)**

8 a. Explain the different layers of the ionosphere. **(06 Marks)**

b. Calculate the critical frequency for F_1, F_2 and E layers for which the maximum ionic densities are 2.3×10^6, 3.5×10^6 and 1.7×10^6 electrons/cm^3 respectively. **(06 Marks)**

c. Describe the significance of MUF and skip distance. Deduce the expression for MUF. **(08 Marks)**

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10EC65

Sixth Semester B.E. Degree Examination, Aug./Sept.2020
Operating Systems

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Briefly explain the different classes of operating systems. Specifying the primary concern and key concepts used. **(10 Marks)**

b. What are common tasks performed by operating system? Explain briefly. **(06 Marks)**

c. Explain two types of resource allocation. **(04 Marks)**

2 a. Discuss operating systems with monolithic structure and the multiprogramming systems. **(10 Marks)**

b. Explain Kernel based and Microkernel based operating system. **(10 Marks)**

3 a. What is thread? Explain the implementation of Kernel-level thread and User-level thread. **(10 Marks)**

b. Explain process states and state transition in Unix. **(06 Marks)**

c. Discus the advantages of child processes. **(04 Marks)**

4 a. Differentiate between :
(i) Static and dynamic memory allocation.
(ii) First fit and Best fit free space allocation **(08 Marks)**

b. Explain merging of free areas using boundary tags. **(08 Marks)**

c. Compare contiguous and non-contiguous memory allocation. **(04 Marks)**

PART – B

5 a. Explain demand loading of pages. **(08 Marks)**

b. For the following page reference string, calculate the number of page faults with LRU when
(i) Number of Page frames are three
(ii) Number of Page frames are four.
Page reference string : 5, 4, 3, 2, 1, 4, 3, 5, 4, 3, 2, 1, 5. **(06 Marks)**

c. Explain address translation in paged virtual memory. **(06 Marks)**

6 a. Explain the organization of sequential access and direct access files. **(08 Marks)**

b. Explain the different operations performed on files. **(04 Marks)**

c. With a neat diagram, explain the facilities provided by file system and IOCS layers. **(08 Marks)**

7 a. Compute mean turn around time and weighted turn around time for following set of processes, using FCFS scheduling:

Processes	P_1	P_2	P_3	P_4	P_5
Arrival time	0	2	3	5	9
Service time	3	3	2	5	3

(06 Marks)

b. Explain Scheduling in Unix. **(08 Marks)**

c. Explain the long term, medium term and short term scheduler. **(06 Marks)**

8 a. Explain (i) direct and indirect naming (ii) blocking and nonblocking sends **(06 Marks)**

b. Write short note on mail box and mention its advantages. **(08 Marks)**

c. With a neat diagram, explain Inter Process Communication in Unix. **(06 Marks)**

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10EC661

Sixth Semester B.E. Degree Examination, Aug./Sept. 2020
Analog and Mixed Mode VLSI Design

Time: 3 hrs. Max. Marks:100

Note: *Answer any FIVE full questions, selecting atleast TWO questions from each part.*

PART – A

1 a. With neat diagram explain sample and word characteristics. **(08 Marks)**

b. With neat diagram explain mixed signal layout issues. **(08 Marks)**

c. Find the number of input combinations values for 1LSB, the percentage accuracy 4 full scale voltage (VFS) generated for 3 bit and 8 bit DAC assuming $V_{REF} = 5V$. **(04 Marks)**

2 a. Design and explain N bit R – 2R ladder network find out total resistance value in horizontal and vertical branches. **(10 Marks)**

b. 3 bit resistor string DAC was designed with derived resistor of 500Ω. After fabrication mismatch caused the actual values of resistors to be $R_1 = 500\Omega$, $R_2 = 480\Omega$, $R_3 = 470\Omega$, $R_4 = 520\Omega$, $R_5 = 510\Omega$, $R_6 = 490\Omega$, $R_7 = 530\Omega$ and $R_8 = 500\Omega$. Determine the maximum INL and DNL for the DAC assuming $V_{ref} = 5V$. **(10 Marks)**

3 a. i) Explain briefly cyclic digital to analog converter. **(06 Marks)**

ii) Explain briefly pipeline digital to analog converter. **(06 Marks)**

b. Explain briefly block diagram of two step flash ADC. **(08 Marks)**

4 a. Explain how level shifter can be used in the operational amplifiers level shifters to avoid, the shift in operating point due to direct coupling between the constructive stages. **(08 Marks)**

b. Explain neat diagram of high performance comparator with each stages. **(12 Marks)**

PART – B

5 a. Explain with neat block diagram of process flow and fabrication steps of submicron CMOS process flow. **(12 Marks)**

b. In the mixed signal IC design explain how MOS device behave as a capacitor. **(08 Marks)**

6 a. Explain how to determine the performance of the data converter SNR. **(10 Marks)**

b. Explain with neat block diagram of working principle of dump and interpolate circuit with ADC. **(05 Marks)**

c. Determine the effective number of bits for an ADC with $V_{ref+} = 1.5V, V_{ref-} = 0$ and a measured V_{QeRMS} of 2mV. **(05 Marks)**

7 a. Explain and write the circuit of, when circuit contains two tristate inverters driven by a clock signal and its inverse and the basic working principles of this circuit is similar and the simple delay element. **(08 Marks)**

b. Explain with neat block diagram of 4 bit pipelined adder. **(06 Marks)**

c. Estimate the high to low and low to high delays in the circuit shown in Fig.Q7(c).

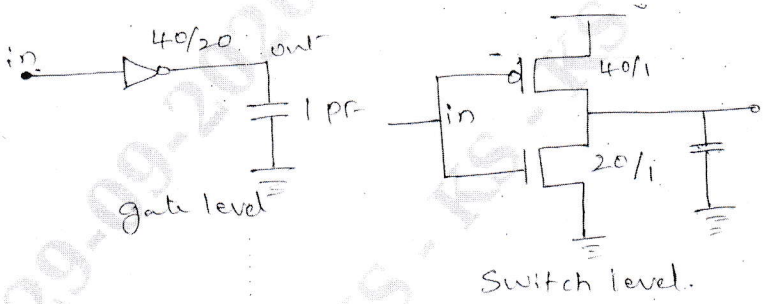

Fig.Q7(c) **(06 Marks)**

8 a. With neat block diagram explain two stage op-amp. **(05 Marks)**

b. With neat sketch of circuits explain the design of mixed op-amp with important parameters. **(15 Marks)**

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10EC662

Sixth Semester B.E. Degree Examination, Aug./Sept.2020
Satellite Communications

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART - A

1 a. List the frequency – band designations which are in common use for satellite services. **(06 Marks)**

b. What is INTELSAT? How it covers the 'international traffic'? **(04 Marks)**

c. State and explain the Kepler's laws of planetary motion, with neat diagram and necessary equations. **(10 Marks)**

2 a. Explain how a satellite continues to be in orbit and derive expression for :
i) Satellite velocity ii) Orbital period. **(08 Marks)**

b. Define and explain Elevation and Azimuth angles of a ground station antenna for communication, with an orbiting satellite. **(06 Marks)**

c. The orbit of an earth orbiting satellite has an eccentricity of 0.15 and semi major axis of 9000 kms. Determine i) Periodic time ii) Apogee height iii) Perigee height. Given $h = 3.986 \times 10^5$ km^3/s^2. Assume a mean value of 6371 kms for earth's radius. **(06 Marks)**

3 a. Explain Atmospheric and Ionospheric losses for satellite communication. **(05 Marks)**

b. For the system given in fig.Q3(b) (i) and (ii), the receiver noise figure is 12dB, cable loss 5dB , LNA gain 50dB and its noise temperature 150K , Antenna noise temperature 35K, calculate noise temperature referred to the input. Conclude the result. **(07 Marks)**

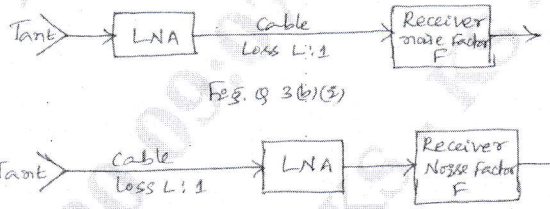

Fig.Q3(b)

c. Calculate rain attenuation for a frequency of 18GHz for circular polarization. The rain height of 2km, a rain rate of 10mm/hr is exceeded for 0.001 percent of the year. The earth station altitude 600m and antenna elevation angle is 35^0 ($a_h = 0.0751$, $a_v = 0.0691$, $b_h = 1.099$, $b_v = 1.065$). **(08 Marks)**

4 a. What is a Satellite transponder? With a neat diagram, explain the overall frequency arrangement of typical C – band communication satellite. **(06 Marks)**

b. With the help of neat diagram, explain the forms of altitude control. **(10 Marks)**

c. Explain TT and C functions with block diagram (Telemetry, Tracking and Command). **(04 Marks)**

PART - B

5 a. With a neat diagram, explain the outdoor and indoor units of a receive – only home TV system. **(10 Marks)**

b. An FM/TV carrier is specified as having a modulation index of 2.571 and a top modulating frequency of 4.2 MHz. Calculate the protection ration required to give a quality impairment factor of (i) 4.2 ii) 4.5. **(04 Marks)**

c. Explain Preassigned FDMA. **(06 Marks)**

6 a. Explain Unique Word detection. Obtain equation for miss probability and false detection probability. **(10 Marks)**

b. The carrier to interference ratio at the ground receiving antenna is 23.3 dB. For the uplink (C/I) ratio is 27.53 db. Find the overall ratio $(C/I)_{ant}$ for $(I/C)_U = 0.001766$ and $(I/C)_D = 0.004436$. **(06 Marks)**

c. What are different interferences that occur in FDMA system? **(04 Marks)**

7 a. Explain i) Transponder capacity ii) Frequency and Polarization. **(08 Marks)**

b. Explain the principles of Global positioning satellite system in detail. **(06 Marks)**

c. Describe the operation of typical VSAT system. **(06 Marks)**

8 Write short notes on :

a. SPADE system.

b. Earth Eclipse of satellites.

c. Transmit – Receive earth stations.

d. Radar sat. **(20 Marks)**

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