CBCS SCHEME

USN | | | | | | | | | | **15EC61**

Sixth Semester B.E. Degree Examination, Aug./Sept.2020
Digital Communication

Time: 3 hrs.   Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1   a.   Define Hilbert transform. State the properties of it. Mention its applications.   **(05 Marks)**
    b.   What is line coding? For binary stream 101001 sketch the following line codes:
         (i) Polar RZ   (ii) Polar NRZ   (iii) Bipolar NRZ   (iv) Manchester   **(05 Marks)**
    c.   Derive the expression for the complex low pass representation of band pass systems.
                                                                                    (06 Marks)

OR

2   a.   Derive the expression for power spectral density of Manchester format and draw the spectrum.   **(06 Marks)**
    b.   Define pre-envelope and complex envelope of a real values signal. Given a band pass signal S(t), sketch the spectral representation of signal S(t), pre-envelope and complex envelope.
                                                                                    (06 Marks)
    c.   Code the binary pattern (i) 1110000101101000000000010 using HDB3 and bipolar NRZ
         (ii) 011000011 using B3ZS. Draw B3ZS waveform.   **(04 Marks)**

Module-2

3   a.   Use Gram-Schmidt orthoganalization procedure and find the set of orthonormal basis functions to represent the four signals $S_1(t)$, $S_2(t)$, $S_3(t)$ and $S_4(t)$ shown in Fig.Q3(a). Also express each of these signals in terms of the set of basis functions.
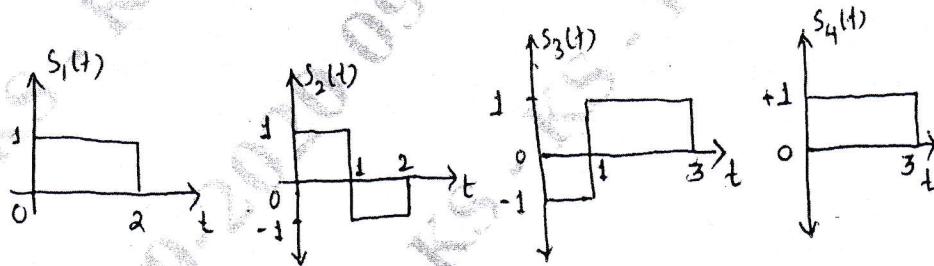

Fig.Q3(a)   **(08 Marks)**
    b.   Explain the matched filter receiver with the relevant mathematical theory.   **(08 Marks)**

OR

4   a.   Explain the geometric representation of signals and express energy of the signal in terms of the signal vector.   **(08 Marks)**
    b.   Explain the operation of correlation receiver with relevant diagrams.   **(04 Marks)**
    c.   Explain how to convert continuous AWGN channel into a vector channel.   **(04 Marks)**

Module-3

5   a.   Explain the BPSK signal with its signal space characterization. With a neat block diagram, explain the generation and detection of BPSK signal.   **(10 Marks)**
    b.   What is difference between BPSK and DPSK? Illustrate the operation of DPSK for the binary sequence 11010101. Assume reference bit as '1'.   **(06 Marks)**

OR

6 a. Derive an expression for probability of error of BFSK. **(06 Marks)**
   b. What is an advantage of M-ary QAM over M-ary PSK system? Obtain the constellation of QAM for M = 4 and draw the signal space diagram. **(04 Marks)**
   c. With a neat diagram, explain the generation and detection of QPSK signals. **(06 Marks)**

Module-4

7 a. With a neat block diagram, explain the digital PAM transmission through band limited baseband channels and obtain the expression for ISI. **(06 Marks)**
   b. State the Nyquist criterion for zero ISI. **(02 Marks)**
   c. What are adaptive equalizers? Explain linear adaptive equalizer based on MSE criterion. **(08 Marks)**

OR

8 a. For the binary data sequence 11101001 given as input to the pre-coder. The output of the pre-coder is used to modulate a duo binary transmitting filter. Obtain the :
      (i) Pre-coded sequence   (ii) Transmitted amplitude levels
      (iii) The received signal levels   (iv) Decoded sequence **(04 Marks)**
   b. Explain the design of band limited signals with controlled ISI. Describe the time domain and frequency domain characteristics of a duo binary signal. **(07 Marks)**
   c. What is channel equalization? With a neat diagram, explain the concept of equalization using a linear transversal filter. **(05 Marks)**

Module-5

9 a. Explain the model of a spread spectrum digital communication system. **(05 Marks)**
   b. With a neat block diagram, explain the CDMA system based on IS-95. **(08 Marks)**
   c. Write a short note on application of spread spectrum in wireless LAN. **(03 Marks)**

OR

10 a. With a neat block diagram, explain frequency hopped spread spectrum technique. Explain the terms chip rate, jamming margin and processing gain. Also mention its applications. **(08 Marks)**
    b. Explain the effect of dispreading on a narrow band interference in DSSS systems. A DSSS is designed to have the power ratio P_R/P_N at the intended receiver is 10^{-2}. If the desired $E_b/N_o = 10$ for acceptable performance, determine the minimum value of processing gain. **(04 Marks)**
    c. Mention the applications of DSSS and explain any one in detail. **(04 Marks)**

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15EC63

Sixth Semester B.E. Degree Examination, Aug./Sept. 2020
VLSI Design

Time: 3 hrs.   Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1 a. Explain the ideal I.V characteristics of nMOS transistor. Derive the equation for I_{DS} in three region   i) cut off region   ii) non–saturated region   iii) saturation region.   **(10 Marks)**
   b. Explain the nMOS fabrication with neat diagram.   **(06 Marks)**

OR

2 a. Explain the CMOS inverter transfer characteristics highlighting the regions of operations of the MOS transistor.   **(06 Marks)**
   b. Describe with heat sketches the fabrication of P-well CMOS inverter.   **(06 Marks)**
   c. Compare CMOS and bipolar technology.   **(04 Marks)**

Module-2

3 a. Draw the circuit schematic and stick diagram of CMOS 2 input NAND gate.   **(08 Marks)**
   b. Explain briefly λ-based design rules for wire and transistor (nMOS, PMOS, CMOS).   **(08 Marks)**

OR

4 a. Explain with diagram rise time model and fall time model of CMOS inverter.   **(06 Marks)**
   b. Explain briefly the circuit of inverting and non-inverting super buffer.   **(06 Marks)**
   c. Explain delay unit τ.   **(04 Marks)**

Module-3

5 a. What are the most commonly used scaling models? Provide scaling factor for :
      i) Power dissipasen per gate   ii) Current density
      iii) Channel resistance Ron   iv) Parasitic capacitance C_x.   **(06 Marks)**
   b. What are the general considerations to be followed in designing a sub system?   **(05 Marks)**
   c. Explain the design steps for 4-bit adder.   **(05 Marks)**

OR

6 a. Design regularity.   **(04 Marks)**
   b. Design 4 bit ALU to implement addition subtraction, EX-OR, EX-NOR and AND operation.   **(12 Marks)**

Module-4

7 a. Discuss the architectural issue related to sub system design.   **(06 Marks)**
   b. Explain briefly a parity generator with block diagram and stick diagram.   **(06 Marks)**
   c. Give the comparison of SSRAM and antifuse FPGA.   **(04 Marks)**

OR

8 a. Explain with schematic view of flash based FPGA.   **(05 Marks)**
   b. Explain briefly switch logic implementing of a four way multiplexer.   **(07 Marks)**
   c. What are the advantages of FPGA?   **(04 Marks)**

Module-5

9 a. Explain the three transistor dynamic RAM – cell.   **(08 Marks)**
   b. Explain briefly nMOS Pseudo static memory cell.   **(08 Marks)**

OR

10 a. Explain briefly logic verification principle.   **(08 Marks)**
    b. Write a short note on : i) Built In Self Test (BIST)   ii) Scan Design Technology.   **(08 Marks)**

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Sixth Semester B.E. Degree Examination, Aug./Sept. 2020
Computer Communication Networks

Time: 3 hrs.   Max. Marks: 80

Note: *Answer any FIVE full questions, choosing ONE full question from each module.*

Module-1

1   a. Outline the functions of various layers in TCP/IP with necessary diagram to show logical connection between layers. **(08 Marks)**
    b. Explain the various services of datalink layer. **(08 Marks)**

OR

2   a. Explain stop and wait protocol. Also explain with necessary diagrams how sequence and acknowledge numbers prevent duplication of frames. **(10 Marks)**
    b. Compare various physical topologies in a computer network. **(06 Marks)**

Module-2

3   a. List the controlled access methods. Also explain reservation access method. **(06 Marks)**
    b. Summarize standard Ethernet implementations. **(04 Marks)**
    c. A pure ALOHA network transmits 200 bit frames on a shared channel of 200 kbps. What is the throughput if the system produces :
       i)   1000 frames per second
       ii) 500 frames per second
       iii) 250 frames per second. **(06 Marks)**

OR

4   a. Explain CSMA/CA protocol with a flow diagram. **(08 Marks)**
    b. Explain Ethernet frame. **(04 Marks)**
    c. A network using CSMA/CD has a bandwidth of 10Mbps. If the maximum propagation time is 25.6μs, what is the minimum size of the frame? **(04 Marks)**

Module-3

5   a. Compare two types of Bluetooth networks and also explain various layers of Bluetooth. **(08 Marks)**
    b. Explain in brief DHCP. **(04 Marks)**
    c. An organization is granted a block of addresses with the beginning address 14·24·74·0/24. The organization needs to have 3 subblocks of addresses to use in its three subnets : one subblock of 10 addresses, one subblock of 60 addresses and one subblock of 120 addresses. Design the subblock. **(04 Marks)**

OR

6   a. Explain in brief various categories of connecting devices. **(06 Marks)**
    b. Explain the following :
       i) QoS
       ii) Congestion control. **(04 Marks)**
    c. Explain with a neat diagram virtual circuit packet switched network. **(06 Marks)**

Module-4

7 a. Explain with a neat diagram IP datagram format. (08 Marks)
   b. Illustrate with an example, Linkstate routing. (08 Marks)

OR

8 a. What is distance vector routing? Explain the various drawbacks of distance vector routing and a few solutions to overcome the same. (08 Marks)
   b. Explain with a diagram three phases of mobile IP. (08 Marks)

Module-5

9 a. Explain with a neat diagram, Goback-n protocol. (08 Marks)
   b. Explain TCP segment format. (08 Marks)

OR

10 a. Explain various services of UDP. (05 Marks)
   b. Compare connection oriented and connectionless services. (08 Marks)
   c. Suppose a TCP connection is transferring a file of 5000 bytes. The first byte is numbered 10001. What are the sequence numbers for each segment if data are sent in five segments, each carrying 1000 bytes? (03 Marks)

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Sixth Semester B.E. Degree Examination, Aug./Sept.2020
Cellular Mobile Communication

Time: 3 hrs.   Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain various capacity expansion techniques with a neat diagram.   **(12 Marks)**
  b. A total of 90 MHz of bandwidth is allocated to FDD cellular telephone system which uses two 30 kHz simplex channels to provide full duplex voice control channels. Compute the number of channels available per cell if a system uses 4 cell reuse.   **(04 Marks)**

OR

2 a. Define trunking and grade of service and explain the call cleared and call delayed.   **(12 Marks)**
  b. Write a short note on log distance path loss model.   **(04 Marks)**

Module-2

3 a. Explain various factors influencing small scale fading.   **(08 Marks)**
  b. Derive an expression for free space propagation model.   **(04 Marks)**
  c. What are different channel assignment strategies and explain the same.   **(04 Marks)**

OR

4 a. Compare Rayleigh and Ricean distribution.   **(06 Marks)**
  b. Explain different types of Small Scale Fading.   **(10 Marks)**

Module-3

5 a. With a neat diagram explain GSM protocol architecture for signaling.   **(10 Marks)**
  b. Explain GSM hyperframe structure with a neat sketch.   **(06 Marks)**

OR

6 a. Explain the GSM traffic and Control signal burst with a neat diagram.   **(10 Marks)**
  b. Explain the GSM speech processing with a neat diagram.   **(06 Marks)**

Module-4

7 a. Explain the location update procedure in GSM system.   **(08 Marks)**
  b. Explain the flow diagram for the outgoing call setup in GSM system.   **(08 Marks)**

OR

8 a. Explain GPRS system architecture and interfaces with a neat sketch.   **(10 Marks)**
  b. List different types of handover techniques in GSM system.   **(03 Marks)**
  c. List different services supported by GSM network.   **(03 Marks)**

Module-5

9 a. Explain various steps involved in call establishment in CDMA system.   **(08 Marks)**
  b. Explain generation of the CDMA paging channel signal with a neat sketch (Block diagram).
                                                                        (08 Marks)

OR

10 a. Explain the reverse access channel processing in a CDMA system with a neat block diagram.   **(10 Marks)**
  b. Explain the Initialization / Registration procedure in CDMA system.   **(06 Marks)**

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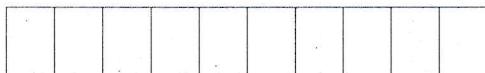
USN |　|　|　|　|　|　|　|　|　|　|　| **15EC663**

Sixth Semester B.E. Degree Examination, Aug./Sept. 2020
Digital System Design using Verilog

Time: 3 hrs.   Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1   a. Develop a verilog model that expresses the logical structure of the gate circuit for vat buzzer. Assume that the sensor signals and the switch signal are inputs to the model, and that the buzzer signal is the output from the model. **(04 Marks)**

    b. Develop a verilog model for a 7-segment decoder. Include an additional input, blank that overrides the BCD input and causes all segments not to be lit. **(06 Marks)**

    c. Develop a data path to perform a complex multiplication of two complex numbers. Whose real and imaginary parts are represented as signed fixed point numbers with 4-pre binary points and 12 post – binary points real and imaginary parts of the product are represented with 8 pre–binary points and 24 post-binary points. Area is the main constraint. **(06 Marks)**

OR

2   a. Explain design methodology followed in IC industry with neat sketch. **(06 Marks)**

    b. Develop a test bench model for the traffic light controller. Verify the conditions that, when the enable input is 1, the output is the same as the light input and when the enable input is '0' all light outputs are inactive. **(04 Marks)**

    c. Write a verilog code for finite state machine of complex multiple control sequence. **(06 Marks)**

Module-2

3   a. Design $1M \times 8$ bit composite memory using $512 k \times 8$ bit memory component. **(04 Marks)**

    b. Determine whether there is an error in the ECC word 000111000100 and if so correct it. **(06 Marks)**

    c. Develop a verilog model of a dual–port, $4K \times 16$ bit flow through SSRAM. One port allows data to be written and read. While the other port only allows data to be read. **(06 Marks)**

OR

4   a. Design a $64k \times 16$ bit composite memory using $16K \times 8$ bit component. **(06 Marks)**

    b. Computer the 12 bit ECC word corresponding to the 8-bit data word 01100001. **(04 Marks)**

    c. Design a FIFO to store upto 256 data items of 16 bits each, using a 256×16 bit dual-port SSRAM for the data storage. The FIFO should provide status outputs, to indicate, when the FIFO is empty and full. Assume that the FIFO will not be read when it is empty, nor be written to when it is full, and that the write and read ports share a common clock. **(06 Marks)**

Module-3

5   a. Outline with a neat sketch, the internal organization of a CPLD. **(06 Marks)**

    b. Design 4-digit decimal counter with seven segment LED display with neat sketch using 74LS390 dual decade counter, four 74LS47 BCD to seven segment decoder, four 7-segment display, plus any additional gates required. **(10 Marks)**

OR

6 a. Outline and explain the internal organization of FPGA. **(08 Marks)**
   b. Explain the concept of differential signaling. How does differential signaling improve noise? **(08 Marks)**

Module-4

7 a. Construct flash ADC and successive approximation ADC with a help of necessary diagram. **(08 Marks)**
   b. Show how a 64-bit data word can be transmitted serially between two ports of a system. Assume that the transmitter and the receiver are both within the same clock domain, and that the signal start is set to 1 on a clock cycle in which data is ready to be transmitted. **(08 Marks)**

OR

8 a. With a net diagram explain R-string DAC and R/2R ladder DAC. **(08 Marks)**
   b. Develop a controller for the keypad matrix and show how to connect the controller to a Gumnut core. Use output port address 4 for the matrix row output register and input address 4 for the matrix column input register. Write the verilog definition for the controller. **(08 Marks)**

Module-5

9 a. Explain the design flow of hardware/software co-design. **(08 Marks)**
   b. Outline the term scan design and boundary scan with neat sketch. **(08 Marks)**

OR

10 a. Demonstrate Built-In Self Test (BIST) techniques. **(08 Marks)**
    b. Illustrate the term design optimization with respect to area, timing and power. **(08 Marks)**

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