Bit interleavers for flexible modulation scheme

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***Abstract*— This paper presents the implementation of bit interleavers in serial concatenated convolution coding scheme. The modulation scheme is flexible, it can be changed from QPSK, 8PSK, 16APSK, 32APSK till 64APSK. As the input data rate is varied the modulation scheme can be changed to adjust to the input data rate. We make use of two convolution coders CC1 and CC2 for encoding of the input data. This encoded data is passed through puncturing system to remove some of the parity bits to achieve the required data rate. Later, the data is passed through the bit interleaver. Interleaving is performed to reduce the effect of errors. Then, after passing through CC2 and puncturing block, the data is finally stored in row-column interleaver. By this we implement the bit interleaver used in flexible modulation scheme.**

***Index Terms*— convolution coding; bit interleaver; puncturing; row-column interleaver; serial concatenated convolution coding**

I. INTRODUCTION

The purpose of this paper is to define an efficient and comprehensive coding modulation solution to support a wide range of spectral efficiency values and data rates.The current specification presents a turbo coding/modulation scheme based on one possible realization of a Serial Concatenated Convolutional Code (SCCC). This scheme makes use of a set of a large variety of modulation techniques (including QPSK, 8PSK, 16APSK, 32APSK, and 64APSK) and a wide range of coding rates. Amplitude and phase-shift keying or asymmetric phase-shift keying (APSK) is a digital modulation scheme that conveys data by changing, or modulating, both the amplitude and the phase of a reference signal (the carrier wave). In other words, it combines both amplitude-shift keying (ASK) and phase-shift keying (PSK) to increase the symbolset. The number of different modulation schemes available, combined with a properly selected coding rate, allows the overall system to make efficient use of the available bandwidth, adapting itself to the variable conditions of the link. The outputs of the binary encoders are mapped to the considered modulation scheme, after being interleaved. In other words, a bit interleaved coded modulation scheme is proposed. The use of SCCC is intended mainly for high data rate applications. The SCCC scheme implies a Physical Layer frame of constant length. This architecture simplifies the synchronization procedure, thus further allowing fast and efficient acquisition at very high rates for the receiver.

II. PRINCIPLE

G. Caire et al. [1] presents the theory underlying bit-interleaved coded modulation, provides tools for evaluating its performance.

S. Benedetto, et al. [2] presents serially concatenated code with interleaver consists of the cascade of an outer encoder, an interleaver permuting the outer codewords bits, and an inner encoder whose input words are the permuted outer codewords. Extensive comparisons with parallel concatenated convolutional codes known as turbo codes are performed, showing that the new scheme can offer superior performance.

O.Y. Takeshita et al. [3], it is presented that an interleaver with random properties, quite often generated by pseudo-random algorithms, is one of the essential building blocks of turbo codes. Interleavers play a critical role in performance of turbo codes.

H.R. Sadjadpour et al. [4], presents the performance of a turbo code with short block length depends critically on the interleaver design. There are two major criteria in the design of an interleaver: the distance spectrum of the code and the correlation between the information input data and the soft output of each decoder corresponding to its parity bits.

R. Garello et al. [5], the basic theory of interleavers is revisited in a semi-tutorial manner, and extended to encompass noncausal interleavers. The parameters that characterize the interleaver behavior (like delay, latency, and period) are clearly defined. The input-output interleaver code is introduced and its complexity is studied. Connections among various interleaver parameters are explored.

Jungpil Yu et al. [6] presents an interleaver design method for SCCC. The design criterion is to minimize the message-round probability in the SCCC graph which is especially well suited for SCCC.

M. Laddomada et al. [7], an effective algorithm for the design of punctured Serially Concatenated Convolutional Codes (SCCCs) is proposed. The algorithm is based on the density evolution technique, and its main goal is to design a code matching the outer and the inner encoder in order to reduce the Bit Error Rate (BER).

Ken Gracie et al. [8], presents that since the introduction of turbo codes in 1993, much more powerful codes referred to collectively as turbo and turbo-like codes have eclipsed classical methods. These powerful error-correcting techniques achieve excellent error-rate performance that can closely approach Shannon's channel capacity limit.

Youssouf Ould-Cheikh-Mouhamedou [9], presents a simple and efficient method for lowering the error floors of turbo codes. This method identifies a set of parity bits that will be forced to take zero bit values when encoding, and exploits these known zero bit parities when decoding.

Francisco J. Escribano et al. [10], presents the well-known property that turbo-like systems owe their success to the principle of reducing error event multiplicities rather than just minimizing related error distances. The increasing need of robust wireless communications, over an already crowded air interface, together with the improvements in hardware and signal processing architectures, is opening the way to the exploitation of new coding and modulation techniques.

Ronald Garzon Bohorquez et al. [11], a method to design channel interleavers based on span properties and mutual information is presented. Resulting interleavers enjoy better burst error control and c mitigate the effect of regular error patterns. For channel interleaving, structures are generated, resulting from a joint optimization of the interleaver span properties in the time and frequency domains. A significant improvement can be observed in severe channel conditions, especially over time and frequencyselective channels with erasures.

Charbel Abdel Nour et al. [12], it is presented that three of the most common interleaver for turbo codes (TCs) are dithered relative prime (DRP) interleavers, quadratic permutation polynomial (QPP) interleavers, and almost relative permutation (ARP) interleavers. In this paper, it is shown that DRP and QPP interleavers can be expressed in the ARP interleaver function. Furthermore, QPP interleavers can be seen a particular case of ARP interleavers, in which values of the periodic shifts follow the quadrant term of the QPP interleaver function.

Yuta Hori et al. [13], it is presented that bit-interleaved coded modulation (BICM), together with orthogonal frequency-division multiplexing (OFDM) signaling, has found its application in many recent wireless standards. BICM-OFDM systems are able to simplify the design of coding and modulation with various information rates for link adaptation.

Manish Yadav et al. [14], it is presented that one of the most popular and effective method adopted for the burst error control is to perform the interleaving operation before the transmission of data over a communication channel. In order to distribute the burst errors, interleaver shuffles the sequence of original message bits. At the receiving end, the received message bits are re-shuffled to recover the message bits in its original sequence. Thus, the selection and designing of appropriate interleavers for an advanced multiple-access technique such as interleave-division multiple-access (IDMA) is always a key challenge.

III. BLOCK DIAGRAM

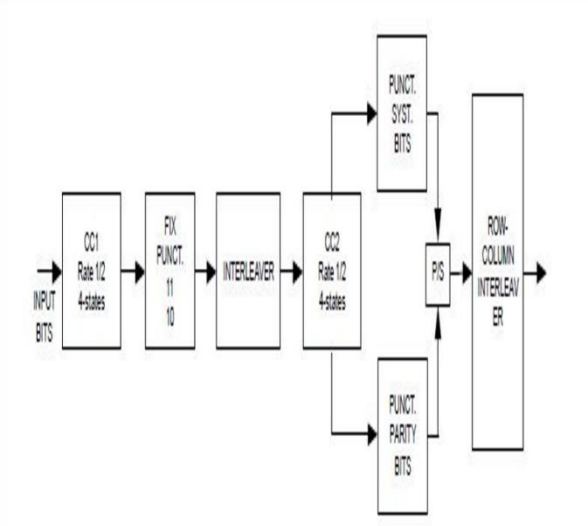

Fig.1: Block diagram of SCCC scheme

The input of 'u' bits is given to the channel encoder 1(CC1). CC1 runs for a total of u+2 bit times producing an output of 2(u+2) encoded bits. The output of the channel encoder is subject to puncturing using a puncturing algorithm.

Puncturing is the process of removing some of the parity bits after encoding with an error correction code. It is performed to obtain the desired coding rate.

Interleaving is the reordering of data that is to be transmitted so that consecutive bits of data are distributed over a larger sequence of data to reduce the effect of errors.

Interleaving is a process or methodology to make a system more efficient, fast and reliable by arranging data in a noncontiguous manner. It helps in storage and

error correction. The use of interleaving greatly increases the ability of error protection codes to correct for errors.

The row-column interleaver is used to pseudorandomize the selection of bits. The data is serially written column-wise and serially read row-wise in a row-column interleaver as shown in Fig 2.

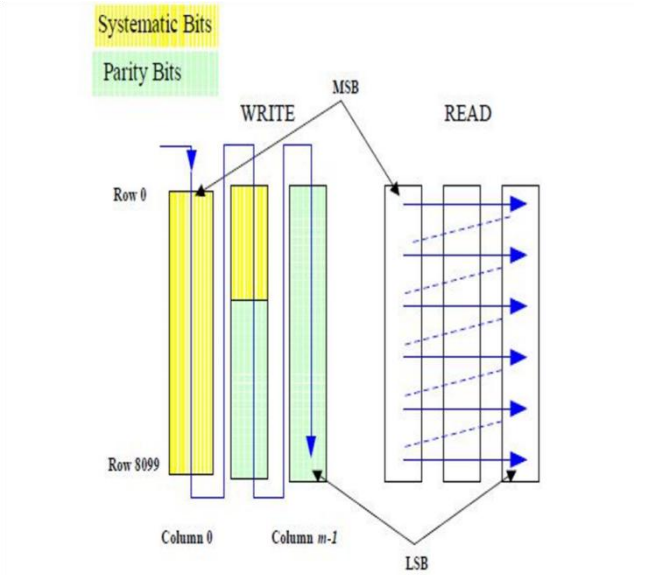

Fig 2: Row-column interleaver

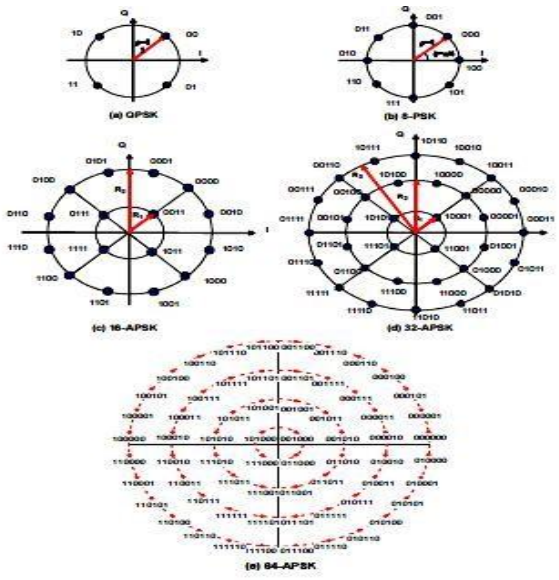

Fig 3: Constellation mapping

In the constellation mapping diagram shown in Fig 3, the 16APSK scheme uses the constellation composed of 2 concentric circumferences, whose number of points shall be set to $N1 = 4$ and $N2 = 12$.

In 32APSK scheme, the constellation is composed of 3 concentric circumferences whose number of points shall be set to $N1 = 4$, $N2 = 12$, and $N3 = 16$.

In 64APSK scheme, the constellation shall be composed of 4 concentric circumferences, whose number of points shall be set to $N1 = 4$, $N2 = 12$, $N3 = 20$, and $N4 = 28$

IV. EXPECTED RESULT

Bit interleaver used in flexible modulation scheme will be designed. For verification purpose, test data has been generated for all interleaving block sizes using MATLAB. Then, the test data has been applied to the VHDL models and the outputs have been compared to the MATLAB results. Finally, for verification of hardware output, the code will be implemented in the FPGA kit.

V. CONCLUSION

By literature review, we have found that the previously used modulation techniques QPSK, 8PSK, 16APSK and 32APSK had bandwidth and power restrictions. So, to overcome the above disadvantage and to get higher modulation, we go for 64APSK. By using 64APSK modulation technique, the error correcting capability can be increased.

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