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10EC/TE71

Seventh Semester B.E. Degree Examination, Dec.2019/Jan.2020
Computer Communication Networks

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART - A

1 a. With a neat diagram, explain TCP / IP Protocol suite with a brief description of the protocol in each layers. **(10 Marks)**

b. Explain cable T.V Networks with a neat diagram. **(06 Marks)**

c. Explain with a neat diagram SS7. **(04 Marks)**

2 a. With a neat diagram, explain three different types of HDLC frames. **(10 Marks)**

b. Apply bit stuffing and unstuffing for
1 0 0 0 1 1 1 1 1 1 1 1 0 0 1 1 1 1 1 0 1 0 0 0 1 1 1 1 1 1 1 1 1 1 0 0 0 0 1 1 1 1 1. **(04 Marks)**

c. Why window size in GO Back N ARQ should be less than 2^m? Explain with an example. **(06 Marks)**

3 a. Describe Polling and Token Passing method under Controlled Access Protocols. **(08 Marks)**

b. In the fig. Q3(b) given , the data rate is 10Mbps, the distance between station A and C is 2000m and the propagation speed is 2×10^8 m/s. Station A starts sending a long frames at time $t_1 = 0$; station C starts sensing a long frame at time $t_2 = 3\mu s$. The size of the frame is long enough to guarantee the detection of collision by both stations. Find
i) The time when station C hears the collision (t_3).
ii) The time when station A hears the collision (t_4).
iii) The number of bits station A has sent before detecting the collision.
iv) The number of bits station C has sent before detecting the collision. **(08 Marks)**

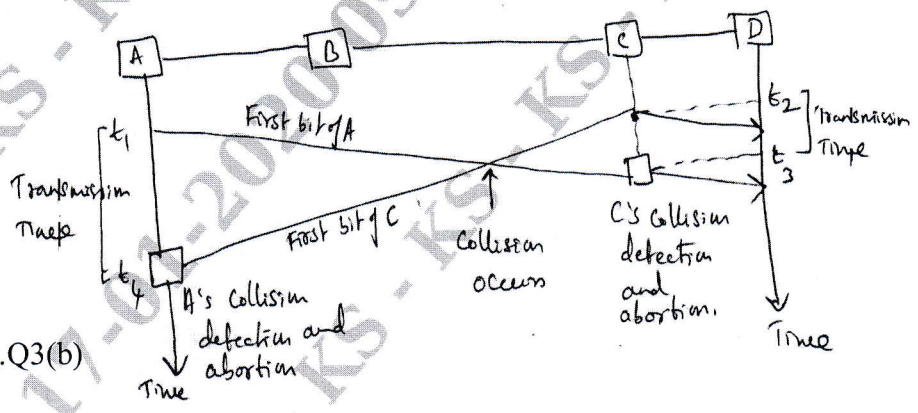

Fig.Q3(b)

c. In a CDMA system the four chip sequences are :
A : (- 1 – 1 – 1 + 1 + 1 – 1 + 1 + 1).
B : (- 1 – 1 + 1 - 1 + 1 + 1 + 1 - 1).
C : (- 1 + 1 – 1 + 1 + 1 + 1 - 1 - 1).
D : (- 1 + 1 – 1 - 1 - 1 – 1 + 1 - 1).
If the received sequence is (-1 + 1 – 3 + 1 – 1 – 3 + 1 + 1) , what is the data transmitted by the four stations. **(04 Marks)**

4 a. What are Hidden and Exposed Station Problems in wireless LANS? Give solution for each. **(10 Marks)**

b. Give the format for IEEE 802.3 Frame format. What are the minimum and Max. Frame length? **(08 Marks)**

c. Identify if the following 802.3 MAC Addresses are Unicast, Multicast or Broadcast.
i) 4A : 30 : 10 : 21 : 10 : 1A ii) 47 : 20 : 1B : 2∈ : 08 : E∈. **(02 Marks)**

PART - B

5 a. Explain three criteria of Transparent bridge in detail with relevant diagrams. **(10 Marks)**

b. A system with Four LANS and Five bridges is shown in fig. Q5(b). Choose B1 as the root bridge. Show the Forwarding and Blocking Ports after applying the spanning tree procedure. **(10 Marks)**

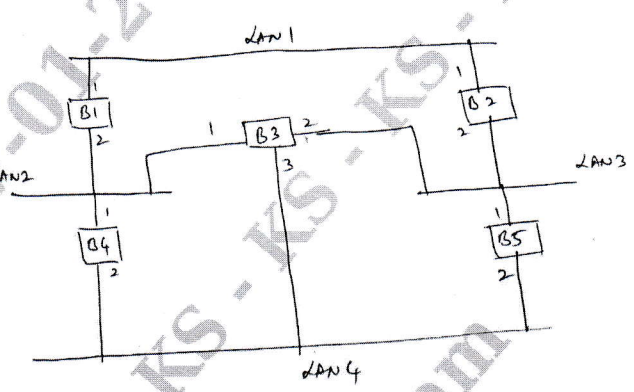

Fig.Q5(b)

6 a. Explain IPV_4 Header Format. **(08 Marks)**

b. Explain briefly strategies used to handle the transition from IPV4 to IPV6. **(06 Marks)**

c. Explain classful addressing and what are the Problems in classful addressing. **(06 Marks)**

7 a. Explain distance vector routing for the following example as shown in fig. Q7(a). **(10 Marks)**

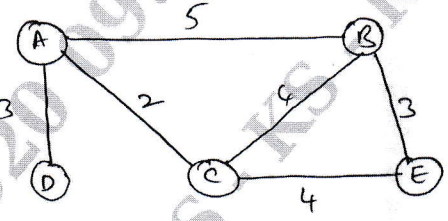

Fig.Q7(a)

b. Compare Multicasting with Multiple Unicasting. Differentiate between source based tree and group shared tree approach used in Multicast routing. **(10 Marks)**

8 a. Describe a TCP connection and explain TCP connection establishment using three way handshaking. **(10 Marks)**

b. Explain Recursive resolution and Iterative resolution in name address resolution. **(10 Marks)**

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10EC/TE72

Seventh Semester B.E. Degree Examination, Dec.2019/Jan.2020
Optical Fiber Communication

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Explain briefly the following :
i) V number or normalized frequency of fiber.
ii) Mode – field diameter (MFD) of a single mode fiber. **(06 Marks)**

b. Explain with a neat diagram, the photonic crystal fibers in optical fiber communication. **(08 Marks)**

c. An optical fiber is air has NA of 0.4. Compare the acceptance angle for meridonal rays with that for skew rays which change direction by 100^0 at each reflection. **(06 Marks)**

2 a. Explain the three different mechanisms that cause absorption of optical energy in optical fibers. **(08 Marks)**

b. What are the types of linear scattering losses and explain them? **(06 Marks)**

c. A 6km optical fiber consists of multimode step – index fiber, with a core refractive index of 1.5 and a relative index difference of 1%, estimate
i) Delay difference between slowest and fastest modes at the fiber output.
ii) rms pulse broadening due to inter – model dispersion on the link.
iii) Maximum bit rate that may be obtained without substantial errors on the line assuming only inter – modal dispersion. **(06 Marks)**

3 a. With a neat diagram, explain the working of an edge emitting LED. Also mention its special features and usage. **(08 Marks)**

b. Give comparison between Laser diode and light emitting diode, considering the various parameters. **(06 Marks)**

c. A double – hetero junction InGaAsP LED emitting at a peak wavelength of 1310 nm has radiative and nonradiative recombination times of 25 and 90ns respectively. The drive current is 35mA.
i) Find the internal quantum efficiency and the internal power.
ii) If the refractive index of the light source material is n = 3.5. Find the power emitted from the device. **(06 Marks)**

4 a. Briefly describe the principle of the operation of the following :
i) Expanded beam connectors ii) Fiber fused biconical taper coupler. **(06 Marks)**

b. Define Fiber Splicing. Explain different types of splicing with sketches. **(08 Marks)**

c. An LED has a circular emitting area of radius 35 μm and a Lambersian pattern with 150 W/cm^2 steradian of axial brightness for a given drive currents out of two step index fibers used, one has core radius 25μm and NA = 0.20 and the other has core radius 50μm and NA = 0.20. Calculate the power coupled to each fiber from the LED and compare. **(06 Marks)**

PART – B

5 a. Explain the receiver sensitivity of an optical receiver. Derive an expression for receiver sensitivity. **(06 Marks)**

b. Explain the general configuration of eye diagram showing the definitions of fundamental measurement parameters. And also explain noise margin and timing fitter parameters. **(09 Marks)**

c. Explain the operation of Burst mode receiver with receiver data pattern and signal level variation in pulses. **(05 Marks)**

6 a. Explain the optical power loss model with a neat diagram. **(08 Marks)**

b. What is RF – over – fiber technique? Explain. **(06 Marks)**

c. What is Frequency Chirping? Bring out its application in a typical optical communication system. **(06 Marks)**

7 a. Explain Operational principle and implementation of WDM with various features. **(08 Marks)**

b. Explain the design and operation of polarization independent isolator. How it is different from polarization dependent isolator? **(06 Marks)**

c. Explain the operation of optical Add/Drop multiplexer with a relevant diagram. **(06 Marks)**

8 a. Explain in detail the amplification mechanism with energy level diagram in an EDFA. **(05 Marks)**

b. Describe i) SONET / SDH rings.
ii) SONET / SDH networks. **(15 Marks)**

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10EC73

Seventh Semester B.E. Degree Examination, Dec.2019/Jan.2020

Power Electronics

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the classification of power semiconductor switching devices, on the basis of control characteristics. **(08 Marks)**

b. Explain different types of power converter systems with circuit and waveforms. **(08 Marks)**

c. Draw symbol and characteristics of the following devices: i) SITH ii) SIT **(04 Marks)**

2 a. Using transient model of BJT, explain switching characteristics of power transistor. **(10 Marks)**

b. The collective clamping circuit in Fig.Q2(b) has V_{CC} = 100 V, R_C = 1.5 Ω, V_{d_1} = 2.1 V, V_{d_2} = 0.9 V, V_{BE} = 0.7 V, V_B = 15 V and R_B = 2.5 Ω, β = 16. Calculate:

i) Collector emitter clamping voltage V_{CE}

ii) Collector event without clamping

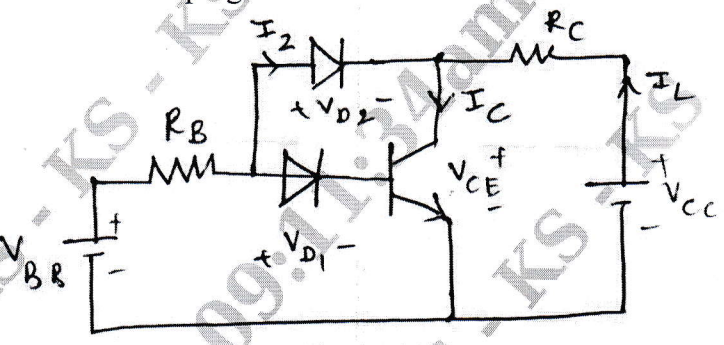

Fig.Q2(b) **(06 Marks)**

c. Compare the features of BJT and MOSFET. **(04 Marks)**

3 a. Using two transistor analogy, derive an expression for anode event of a SCR. **(08 Marks)**

b. Briefly explain dynamic turn-ON and turn-off characteristics of SCR. **(08 Marks)**

c. If the latching event of SCR shown in Fig.Q3(c) is 4 mA, find the minimum width of gate pulse required to turn-ON SCR.

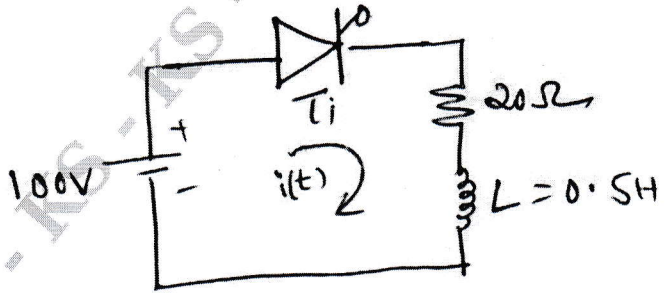

Fig.Q3(c) **(04 Marks)**

4 a. The converter circuit shown in Fig.Q4(a) has resistive load of R and delay angle is $\alpha = \frac{\pi}{2}$, determine:
(i) Rectifier efficiency
(ii) Form factor FF
(iii) Ripple factor RF
(iv) Transformer utilization factor TUF
(v) PIV of thyristor.

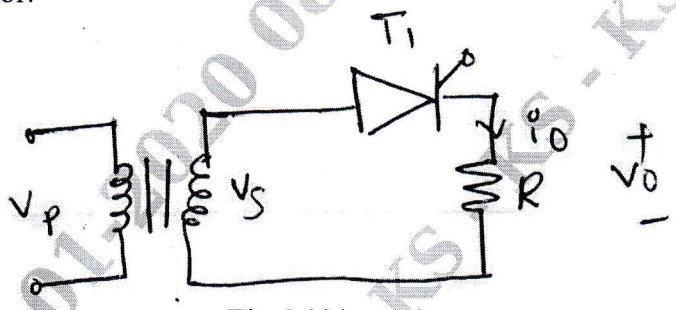

Fig.Q4(a) **(10 Marks)**

b. Explain with neat circuit and waveform, single phase full converter with R-load. Derive equation for V_{DC} and V_{rms}. **(10 Marks)**

PART – B

5 a. Explain the principles of self commutation circuit with necessary circuit and waveform. Derive equation for capacitor voltage and current. **(10 Marks)**

b. The commutation circuit in Fig.Q5(b) has C = 30 μF and inductance L = 4 μH. The initial capacitor voltage is V_D = 200 V. Determine the circuit turn-off time t_{off} if load current I_m is (i) 250 A (ii) 50 A.

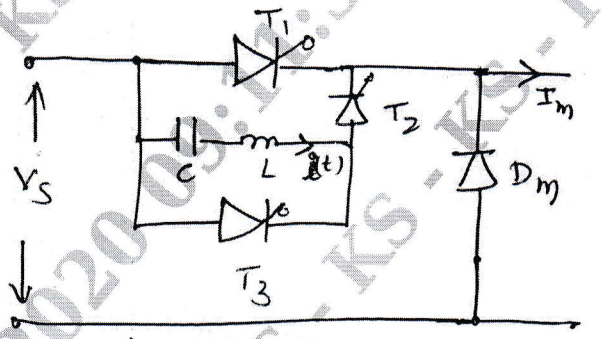

Fig.Q5(b) **(10 Marks)**

6 a. Explain the basic principles of phase angle controller with neat circuit and waveform. Derive equations for RMS and average output voltage. **(10 Marks)**

b. Explain with circuit and waveform, single phase bidirectional controller with resistive loads. Derive equation for RMS output. **(10 Marks)**

7 a. Explain with circuit and waveform, principles of step down chopper with R-load. Derive equation for output voltage. **(10 Marks)**

b. Mention the classification of choppers. Briefly explain each type. **(10 Marks)**

8 a. Explain with circuit and waveform, single phase bridge inverter. **(10 Marks)**

b. Explain with circuit and waveform, single phase current source inverter. **(10 Marks)**

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10TE73

Seventh Semester B.E. Degree Examination, Dec.2019/Jan.2020
Wireless Communication

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART –.A

1 a. List out the differences between 1G & 2G cellular systems. **(05 Marks)**

b. Explain the need of supervisory audio tones and signaling tones for the AMPS system. **(05 Marks)**

c. List out the characteristics of 3G cellular system. **(08 Marks)**

d. What is station class mark? **(02 Marks)**

2 a. Explain the functions and types of RBS system. **(06 Marks)**

b. What is the function of the transcoder controller? **(04 Marks)**

c. Explain the purpose of,
(i) Location area identity (ii) Cell global identity (iii) Global title
(iv) MSISDN (v) IMEI **(10 Marks)**

3 a. Explain the following cellular system capacity expansion techniques:
(i) Cell splitting (ii) Cell sectoring (iii) Lee's microcell technology. **(12 Marks)**

b. Explain the location management. **(08 Marks)**

4 a. Explain with neat diagram the GSM protocols and signaling model. **(08 Marks)**

b. Explain the various logical channels used in GSM. **(06 Marks)**

c. Explain the various GSM traffic and control signal bursts used in GSM. **(06 Marks)**

PART – B

5 a. Explain the GSM traffic channel assignment. **(08 Marks)**

b. Explain the Inter-MSC handover in GSM. **(12 Marks)**

6 a. With a neat block diagram, explain the network nodes found in a CDMA 2000 wireless system. **(10 Marks)**

b. Explain with a neat block diagram, the generation of the CDMA forward traffic / power control channel for 9.6 kbps traffic. **(10 Marks)**

7 a. What is the received power in dBm for a signal in free space with a transmitting power of 1 W, frequency of 1900 MHz and distance from the receiver of 1000 meters if the transmitting antenna and receiving antennas both use dipole antennas with gains of approximately 1.6? What is the path loss in dB? **(04 Marks)**

b. Explain with neat figure the various steps of GSM channel encoding for voice traffic. **(08 Marks)**

c. Explain with neat block diagram the function of a Rake receiver. **(08 Marks)**

8 a. Describe the differences between wireless LAN and wireless PAN technologies. **(12 Marks)**

b. Describe Blue tooth wireless PAN Adhoc network topologies. **(08 Marks)**

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10EC74

Seventh Semester B.E. Degree Examination, Dec.2019/Jan.2020

Embedded System Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. With block diagram, explain the various components in a microprocessor based Embedded System. **(08 Marks)**

b. With diagram, explain Embedded System life cycle. **(08 Marks)**

c. Explain a scheme to interface Embedded system to external world using I/O portion of Von Neumann machine. **(04 Marks)**

2 a. Give the high level block diagram for a FSM and explain the concept. **(05 Marks)**

b. With diagram, explain the DSP architecture used in Embedded System. **(05 Marks)**

c. Explain different types of Execution flow of instruction in an Embedded System. **(05 Marks)**

d. Give the timing diagram for register operations. **(05 Marks)**

3 a. Give the design for a 4k × 16 SRAM. **(08 Marks)**

b. With block diagram, explain basic concepts of caching. **(08 Marks)**

c. With diagram, explain Refresh Timing and Refresh address in DRAM. **(04 Marks)**

4 a. With diagram, explain the water fall model and V cycle model. **(10 Marks)**

b. Explain Architectural design with the help of an example. **(10 Marks)**

PART – B

5 a. Explain the functions of an RTOS. **(10 Marks)**

b. Explain the memory management scheme of an RTOS. **(06 Marks)**

c. What is thread? Explain single process multiple threads. **(04 Marks)**

6 a. Explain Runtime stack, Application stack and Multiprocessing stacks. **(06 Marks)**

b. Give the details of Task control block and explain. **(04 Marks)**

c. Explain operating system virtual machine model and High level OS Architecture with the help of diagrams. **(10 Marks)**

7 a. With the help of memory map, explain memory loading. Also give the design of memory map. **(08 Marks)**

b. Give methods to reduce response time and time loading. **(08 Marks)**

c. Explain Hardware accelerators. **(04 Marks)**

8 a. Analyse the following basic flow control constructs:
(i) Constant time statements (ii) Looping constructs (iii) Conditional statements. **(08 Marks)**

b. Explain the efficiency measures of an Embedded System. **(08 Marks)**

c. Explain SMART cache. **(04 Marks)**

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10TE74

Seventh Semester B.E. Degree Examination, Dec.2019/Jan.2020
DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Explain the issues to be considered in designing and implementing a DSP system. **(06 Marks)**

b. The sequence x(n) = [0 2 4 6 8] is interpolated using an interpolation filter b_k = [0.5 1 0.5] with interpolation factor 2. Determine the interpolation sequence. **(06 Marks)**

c. Explain a digital signal processing system with the help of a block diagram. **(08 Marks)**

2 a. Suggest a scheme to implement a multiplier to multiply two unsigned number using 4×4 Braun multiplier as the building block. **(06 Marks)**

b. What is meant by circular addressing mode? Write pointer updated algorithm for the circular addressing mode and show different cases that encounter during the updating process of the pointer **(06 Marks)**

c. Draw the block diagram to implement 8-tap FIR filter using (i) 8 MAC unit (ii) 2 MAC unit and compare the performance. **(08 Marks)**

3 a. With a help of functional diagram, explain about Multiplier / Adder unit of TMS320C54XX processor. **(06 Marks)**

b. With the block diagram explain the direct addressing mode of TMS320C54XX processor. **(06 Marks)**

c. Explain the PMST register. **(08 Marks)**

4 a. Describe the operation of the following instrumentations of TMS320C54XX processors with an example:
(i) MPY #01234, A (ii) MPY *AR2$^-$, *AR4 + 0, B
(iii) MAC *AR5+, #1234h, A (iv) MAS *AR_3^-, *AR_4 +, B **(08 Marks)**

b. Explain the six stages pipelined execution of TMS320C54XX processor. **(06 Marks)**

c. Write an ALP of TMS320C54XX process to compute sum of three product terms given by the equation y(n) = h(0)x(n) + h(1) x(n – 1) + h(2) x(n – 2) using direct addressing mode where h(0), h(1) and h(2) are stored in data memory location h and x(n), x(n – 1) and x(n – 2) are stored in data memory location x. y(n) is saved in data memory location y and y + 1. **(06 Marks)**

PART – B

5 a. Represent each of the following as 16-bit numbers in the desired Q-notation
(i) 0.35 in Q_{15} (ii) – 0.1958 in Q_{15} (iii) 4000h in Q_{15} (iv) 4000h in Q_7 **(06 Marks)**

b. Write a TMS320C54XX program that illustrate the multiplication of two Q_{15} number to produce Q_{15} result. Write comments. **(06 Marks)**

c. Write an ALP to implement FIR filter. **(08 Marks)**

6 a. Explain how scaling prevents overflow condition in the butterfly computation. Draw the optimum scaling factor for the DIT-FFT butterfly. **(10 Marks)**

b. Explain how the bit reversal index generation can be done in 8-point FFT. Also write a TMS320C54XX subroutine program for 8 point DITFFT bit reversal index generation with comment. **(10 Marks)**

7 a. Draw the memory interface signals for a read-read-write sequence of operations and also explain the signals that are involved. **(06 Marks)**

b. Describe DMA with respect to TMS320C54XX processor. **(08 Marks)**

c. Draw the flow chart of the interrupt handling by the C54XX processor and explain. **(06 Marks)**

8 a. Explain with a neat diagram the operation of the pitch detector. **(10 Marks)**

b. Draw the block diagram of JPEG encoder and decoder and also explain how JPEG encoding and decoding is implemented in DSP. **(10 Marks)**

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10EC751

Seventh Semester B.E. Degree Examination, Dec.2019/Jan.2020
DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO full questions from each part.***

PART – A

1 a. With a neat block diagram, explain the issues to be considered in designing and implementing a DSP system. **(04 Marks)**

b. With a neat block diagram, explain the methods of sampling rate conversions in DSP system. And if the sequence x(n) = [0, 4, 8, 12, 16] is interpolated using interpolation sequence b_k = [1/4, 2/4, 3/4, 2/4, 1/4] and the interpolation factor is 4. Find the interpolated sequence y(m). **(16 Marks)**

2 a. Draw and explain 4 × 4 Braun multiplier structure. What is the total propagation delay if each adder introduces 1.4 units of delay? **(07 Marks)**

b. What is meant by circular addressing mode? Write pointer updating algorithm for the circular addressing mode and show different cases that encounter during updating process of the pointer. **(08 Marks)**

c. Explain implementation of a 16-tap FIR filter, using two MAC units (parallel). Draw its block diagram. **(05 Marks)**

3 a. Compare architectural features of TMS320C25 and ADSP2100 fixed point digital signal processor. **(06 Marks)**

b. Write an explanatory note on direct addressing mode of TMS320C54XX processor. **(10 Marks)**

c. Assuming the current contents of AR3 to be 0200h, what will be its contents after each of the following TMS320C54XX addressing modes is used? Assume that the contents of ARO is 0020h.

i) *AR3 + 0
ii) *+AR3 (40h)
iii) *AR3-
iv) *AR3 **(04 Marks)**

4 a. Describe with a neat block diagram, the operation of hardware timer in TMS320C54XX DSP's. **(10 Marks)**

b. Show the pipeline operation of the following sequence of instructions if the initial values of AR1, AR3, A are 84, 81, 1 and the values stored in memory location 81, 82, 83, 84 are 2, 3, 4, 6. Also provide the values of registers AR3, AR1, T and accumulator, A, after completion of each cycle.

```
ADD *AR3+, A
LD *AR1+, T
MPY *AR3+, B
ADD B, A
  ⋮
```

(10 Marks)

PART – B

5 a. Determine the value of each of the following 16-bit numbers represented using the given Q-notations:
   i) 4400h as a Q0 number
   ii) 4400h as a Q7 number
   iii) -0.3125 as a Q15 number
   iv) -352 as a Q0 number **(04 Marks)**

b. Write an assembly language program for TMS320C54XX processor to multiply two Q15 numbers to produce Q15 number result. **(06 Marks)**

c. Explain how FIR filter can be implemented using TMS320C54XX processor. **(10 Marks)**

6 a. Determine the following for a 512-point FFT computation:
   i) Number of stages
   ii) Number of butterflies in each stage
   iii) Number of butterflies needed for the entire computation
   iv) Number of butterflies that needed no twiddle factors
   v) Number of butterflies that require real twiddle factors
   vi) Number of butterflies that require complex twiddle factors. **(06 Marks)**

b. Explain how scaling prevents overflow condition in the butterfly computation. Derive the optimum scaling factor for the DIT-FFT butterfly. **(10 Marks)**

c. Write the structure of an 8-point DIT-FFT implementation. Take scaling factor for all butterflies as (1/4). **(04 Marks)**

7 a. Design a data memory system with address range 000800h – 000FFFh for a C5416 processor using 2k × 8 SRAM memory chips. **(06 Marks)**

b. Explain an interface between an A/D converter and the TMS320C54XX processor in the programmed I/O mode. **(06 Marks)**

c. Describe DMA with respect to TMS320C54XX processors. **(08 Marks)**

8 a. Explain PCM3002 CODEC, with the help of a neat block diagram. **(10 Marks)**

b. With the help of a block diagram, explain the image compression and reconstruction using JPEG encoder and decoder. **(10 Marks)**

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10TE754

Seventh Semester B.E. Degree Examination, Dec.2019/Jan.2020
Image Processing

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Explain the components of a general purpose image processing system with a neat block diagram. **(08 Marks)**

b. Describe the formation of image in an human eye with a neat sketch and illustration. **(08 Marks)**

c. List the applications of image processing. **(04 Marks)**

2 a. Explain the image acquisition with sensor arrays. **(08 Marks)**

b. Define image sampling and quantization. Explain the basic concepts with an example. **(08 Marks)**

c. How many minutes would it take to transmit a 1024 × 1024 image with 256 gray levels using 56K band modem. Assume, a packet consists of one start and one stop bit. **(04 Marks)**

3 a. Calculate the transformed image V and basis images.

$$A = \frac{1}{\sqrt{2}}\begin{bmatrix}1 & 1\\ 1 & -1\end{bmatrix} \quad V = \begin{bmatrix}1 & 2\\ 3 & 4\end{bmatrix}.$$ **(06 Marks)**

b. List the properties of unitary transforms and explain any 2 properties. **(06 Marks)**

c. List the properties of 2D –DFT and prove any 2 properties. **(08 Marks)**

4 a. Define discrete sine transform. List any 5 properties. **(06 Marks)**

b. Develop Hadamard transform for n = 3. Write 4 properties. **(08 Marks)**

c. Construct Haar transform matrix for n = 2. **(06 Marks)**

PART – B

5 a. Define "Image Enhancement". Explain basic gray level transformations in spatial domain. **(08 Marks)**

b. For the given 4 × 4 image having gray scale between [0 –9] get histogram equalized image. Draw the histogram of image before and after equalization.

3	6	6	3
8	3	8	6
6	3	6	9
3	8	3	8

(06 Marks)

c. Explain image subtraction and image averaging operations with examples. **(06 Marks)**

6 a. Explain the basic steps for filtering in the frequency domain. Mention its advantages. **(06 Marks)**

b. Explain sharpening of images in frequency domain using : i) ideal high pass filter ii) Butterworth high pass filter. **(08 Marks)**

c. Explain homomorphic filtering approach with a neat block diagram. **(06 Marks)**

7 a. Explain inverse filtering approach and its limitations in image restoration. (06 Marks)
b. List the various noise probability density functions along with mathematical expressions and graphs. (08 Marks)
c. Discuss the importance of adaptive median filter and highlight the working of adaptive median filters in image restoration. (06 Marks)

8 a. Develop a scheme for converting colors from : i) RGB to HIS ii) HIS to RGB. (10 Marks)
b. Explain the following pseudo image processing techniques. I) intensity slicing ii) graylevel to color transformations and their applications. (10 Marks)

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Seventh Semester B.E. Degree Examination, Dec.2019/Jan.2020

Image Processing

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Define a digital image. With neat diagram, explain the components of image processing system. **(10 Marks)**

b. Briefly explain:
   i) Brightness adaptation and discrimination
   ii) Weber ratio
   iii) Mach bands **(10 Marks)**

2 a. Explain in detail the image acquisition using the three principal sensor arrangements. **(10 Marks)**

b. Consider the two image subsets, S_1 and S_2, shown in the Fig.Q2(b). For V = {1}, determine and explain whether these are (i) 4-adjacent (ii) 8-adjascent (iii) m-adjacent.

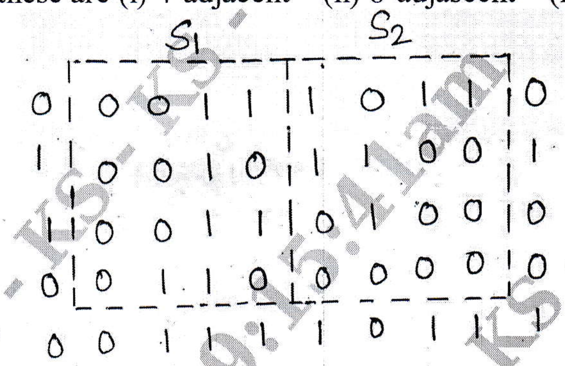

Fig.Q2(b) **(06 Marks)**

c. Consider the image shown in Fig.Q2(c). Let V = {1, 2}
   (i) compute length of shortest m-path
   (ii) compute D_4 distance between the points p and q.

3	0	2	1	1(q)
2	2	0	2	2
1	2	1	1	1
(p)1	0	1	2	2

Fig.Q2(c) **(04 Marks)**

3 a. Define unitary transforms. Explain the properties of unitary transforms. **(06 Marks)**

b. Calculate the transformed image V and the basis images for the orthogonal matrix A and image U.

$$A = \frac{1}{\sqrt{2}}\begin{pmatrix} 1 & 1 \\ 1 & -1 \end{pmatrix} \qquad U = \begin{pmatrix} 2 & 3 \\ 1 & 2 \end{pmatrix}$$ **(06 Marks)**

c. Explain in brief the following properties of 2D – Discrete Fourier Transforms:
   (i) Separability (ii) Translation **(08 Marks)**

4 a. Define 2-D forward and inverse discrete cosine transform, and mention its properties. (08 Marks)

b. Generate 8 × 8 Hadamard transform matrix. The core matrix $H_1 = \frac{1}{\sqrt{2}}\begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}$ indicate its sequency. (04 Marks)

c. Explain Haar transformation with its properties. Compute Haar transformation of image $F = \begin{bmatrix} 3 & -1 \\ 6 & 2 \end{bmatrix}$. (08 Marks)

PART – B

5 a. With necessary graphs, explain the spatial enhancement operations:
   i) Power law transformation
   ii) Gray level slicing
   iii) Contrast stretching
   iv) Bit plane slicing (12 Marks)

b. Derive the equation for histogram equalization. (08 Marks)

6 a. Explain with a block diagram, the basic steps for image filtering in frequency domain. (08 Marks)

b. Explain highpass butterworth filter. (06 Marks)

c. List the steps involved in homomorphic filtering. (06 Marks)

7 a. Explain the basic model for image degradation/restoration process. (06 Marks)

b. Explain inverse filtering with necessary equations. (06 Marks)

c. Explain any four noise models with necessary equations and graphs. (08 Marks)

8 a. Explain different color models. (10 Marks)

b. Explain pseudo coloring. (06 Marks)

c. How many minutes it will take to transmit a 1024 × 1024 colour image with 256 shades of RGB. Assume 56 Kbps modem is used for transmission? (04 Marks)

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USN | | | | | | | | | | 10TE765

Seventh Semester B.E. Degree Examination, Dec.2019/Jan.2020

Embedded System Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. With a neat diagram, describe microprocessor based embedded system. **(10 Marks)**
b. Draw and explain embedded system development life cycle. **(10 Marks)**

2 a. Describe four major blocks of an embedded hardware core. **(06 Marks)**
b. Define addressing modes and explain register direct and indirect addressing modes with necessary diagrams. **(08 Marks)**
c. With a neat diagram, explain ALU. **(06 Marks)**

3 a. List and explain the various types of memories. **(06 Marks)**
b. Draw and explain DRAM inside design using read and write timing diagrams. **(08 Marks)**
c. Explain an associative mapping cache implementation. **(06 Marks)**

4 a. With a neat diagram, explain Waterfall model and spiral model. **(10 Marks)**
b. Explain the system design specifications in an embedded system with an example. **(10 Marks)**

PART – B

5 a. Differentiate between:
i) Program and process
ii) Process and threads
iii) Light weighted and heavy weighted threads **(06 Marks)**
b. Discuss the functions and services of embedded operating system. **(10 Marks)**
c. Explain any two categories of multi-tasking OS. **(04 Marks)**

6 a. Draw and explain virtual machine model operating system architecture. **(06 Marks)**
b. Define TCB and explain the major components of TCB. **(06 Marks)**
c. List and explain the types of stacks. **(08 Marks)**

7 a. Determine the unknown parameter for the system with the following characteristics. The task to be analyzed and improved currently executes in 100 time units and the goal is to reduce execution time to 50 time units. The algorithm to be improved uses 40 time units. Write the inference. **(06 Marks)**
b. Write and analyze linear search algorithm. **(06 Marks)**
c. Write a C program to determine the sum of the elements in an array and obtain complexity function for the same. **(08 Marks)**

8 Write short notes on the following:
a. Memory loading **(08 Marks)**
b. Performance optimization **(06 Marks)**
c. Hardware accelerators **(06 Marks)**

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