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15EC61

Sixth Semester B.E. Degree Examination, Dec.2019/Jan.2020
Digital Communication

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Define Hilbert transform. State the properties of it. **(04 Marks)**

b. Obtain the Hilbert transform of

i) $x(t) = (\cos 2\pi Ft + \sin 2\pi Ft)$

ii) $x(t) = c^{-j2\pi Ft}$ **(04 Marks)**

c. Explain canonical representation of band pass signal. **(08 Marks)**

OR

2 a. Derive the expression for the complex low pass representation of bandpass systems. **(08 Marks)**

b. For the given data stream 11011100. Sketch the line code

i) Unipolar NRZ

ii) Polar NRZ

iii) Unipolar RZ

iv) Bipolar NRZ **(04 Marks)**

c. Draw the power spectra of NRZ unipolar and NRZ polar format. **(04 Marks)**

Module-2

3 a. Show that the energy of a signal is equal to squared length of the signal vector. **(08 Marks)**

b. Obtain the decision rule for maximum likelihood decoding and explain the correlation receiver. **(08 Marks)**

OR

4 a. Explain the correlation receiver using product integrator and matched filter. **(08 Marks)**

b. Three signals $s_1(t)$, $s_2(t)$ and $s_3(t)$ are shown in Fig.Q.4(b). Apply Gram Schmidt procedure to obtain an orthonormal basis for the signals. Express signals $s_1(t)$, $s_2(t)$ and $s_3(t)$ in terms of orthonormal basis functions. **(08 Marks)**

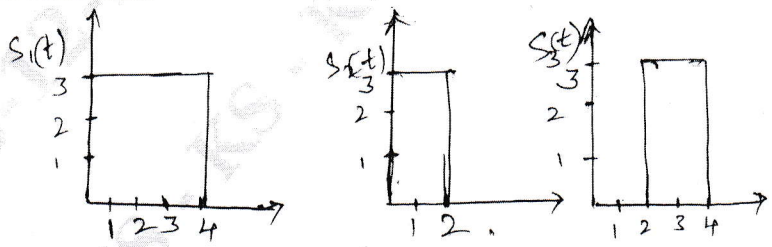

Fig.Q.4(b)

Module-3

5 a. With necessary diagrams, explain the generation and reception of BPSK signal. **(10 Marks)**

b. Given the binary data 10010011, draw the BPSK and DPSK waveforms. **(06 Marks)**

OR

6 a. Derive the expression for error probability of BFSK. **(08 Marks)**

b. With block diagram explain generation and detection of DPSK. **(08 Marks)**

Module-4

7 a. What is ISI? Obtain the expression of output of a filter with intersymbol interference. **(08 Marks)**

b. Explain the Nyquist criterion for distortionless baseband binary transmission and obtain the ideal solution for zero ISI. **(08 Marks)**

OR

8 a. Draw and explain the time-domain and frequency domain of duobinary and modified duobinary signal. **(08 Marks)**

b. What is channel equalization? With a neat diagram, explain the concept of equalization using a linear transversal filter. **(08 Marks)**

Module-5

9 a. Draw the 4 stage linear feedback shift register with 1st and 4th state is connected to Modulo-2 adder. Output of Modulo-2 is connected to 1st stage input. Find the output PN sequence and write the autocorrelation function with initial state 1000. **(06 Marks)**

b. Explain the generation of direct sequence spread spectrum with relevant waveforms and spectrums. **(07 Marks)**

c. Write a short note on application of spread spectrum in wireless LAN's. **(03 Marks)**

OR

10 a. With necessary block diagram, explain the transmitter and receiver of frequency hop spread spectrum. **(08 Marks)**

b. With a neat block diagram, explain the CDMA system based on IS-95. **(08 Marks)**

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15EC62

Sixth Semester B.E. Degree Examination, Dec.2019/Jan.2020
ARM Microcontroller & Embedded Systems

Time: 3 hrs. Max. Marks: 80

Note: ***Answer FIVE full questions, choosing one full question from each module.***

Module-1

1 a. Explain the architecture of ARM cortex – M3 processor with the help of neat block diagram. **(10 Marks)**

b. List and explain the features of ARM cortex M3 processor. **(06 Marks)**

OR

2 a. Explain the operation modes and privilege levels in cortex M3 processor. **(08 Marks)**

b. Explain two stack model and reset sequence in ARM cortex M3. **(08 Marks)**

Module-2

3 a. Explain the following instruction with examples:
(i) ASR (ii) LSL (iii) ROR (iv) REV **(08 Marks)**

b. Briefly explain bit band operations and memory map of cortex M3. **(08 Marks)**

OR

4 a. Write a note on barrier instruction in cortex M3. **(06 Marks)**

b. With a diagram, explain the organization of CMSiS and its benefits. **(10 Marks)**

Module-3

5 a. Define embedded systems. Explain the 6 purpose of embedded systems with an example for each. **(08 Marks)**

b. Explain the classification of embedded systems based on generation. **(04 Marks)**

c. Mention the application of embedded system with an example for each. **(04 Marks)**

OR

6 a. Explain the different 'on board' communication interfaces in brief. **(08 Marks)**

b. Write a note on: (i) Reset circuit (ii) Watch dog timer. **(08 Marks)**

Module-4

7 a. Explain the different characteristics of embedded system in detail. **(08 Marks)**

b. With a block diagram, mention the components and in the design of a washing machine and also explain its working. **(08 Marks)**

OR

8 a. What is hardware and software co-design? Explain the fundamental design approaches in detail. **(10 Marks)**

b. With FSM model, explain the design and operation of automatic tea/coffee lending machine. **(06 Marks)**

Module-5

9 a. Define process. Explain in detail the structure, memory organization and state transitions of the process. **(08 Marks)**

b. Explain multi processing, multi tasking and multi programming. **(08 Marks)**

OR

10 a. Explain the simulator and emulator. **(08 Marks)**

b. Write a note on message passing. **(08 Marks)**

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15EC63

Sixth Semester B.E. Degree Examination, Dec.2019/Jan.2020
VLSI Design

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the step-by-step CMOS P-Well fabrication process. **(08 Marks)**

b. With the mathematical equations, explain velocity saturation and mobility degradation effect due to increase in saturation current. **(08 Marks)**

OR

2 a. With the transfer characteristic of skewed inverter, explain the beta ratio effects. **(06 Marks)**

b. Compare CMOS and bipolar technologies. **(06 Marks)**

c. Consider the nMOS transistor in a 180 nm process with a nominal threshold of 0.4V and doping level of 8×10^{17} cm^{-3}. The body is tied to ground with a substrate contact. How much does the threshold change at room temperature if the source is at 1.1V instead of '0'? **(04 Marks)**

Module-2

3 a. Discuss the λ-based design rules (i) Butting contact (ii) Transistors (nMOS, pMOS and CMOS) **(08 Marks)**

b. Derive the expression of delay interms of τ for CMOS inverter pair. **(08 Marks)**

OR

4 a. Draw the layout for $\overline{Y} = A + BC$ using CMOS. **(08 Marks)**

b. Find the C_{in} for the layout shown in Fig.Q4(b).

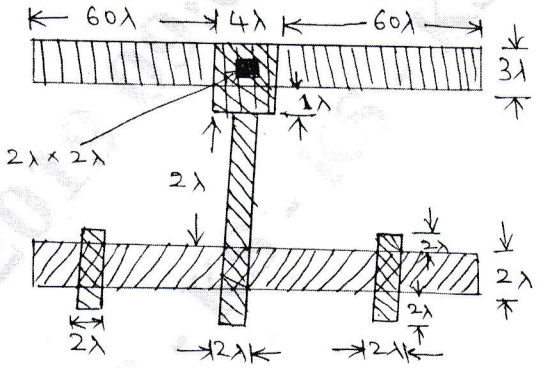

Fig.Q4(b) **(08 Marks)**

Module-3

5 a. Define scaling. Explain the scaling factors for device parameters. **(08 Marks)**

b. What is Manchester Carry Chain? Explain it. **(08 Marks)**

OR

6 a. What are the problems associated with VLSI design and how to reduce by using standard practice? **(06 Marks)**

b. Draw the 4 × 4 cross bar switch using MOS switches and explain it. **(06 Marks)**

c. Calculate the Regularity for 4 × 4 bit and 8 × 8 bit shifter. **(04 Marks)**

Module-4

7 a. Construct a stick diagram for an nMOS parity generator as shown in Fig.Q7(a). The required response is such that z = 1 if there is an even number (including zero) of 1s on the input and z = 0 if there is an odd number.

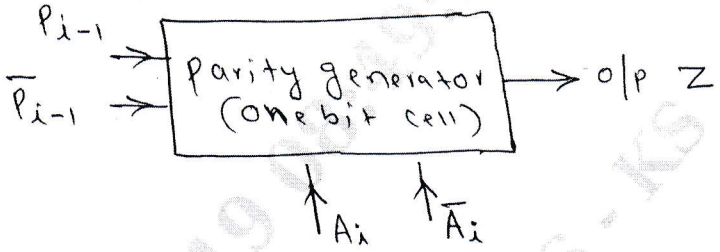

Fig.Q7(a) **(08 Marks)**

b. Draw the block diagram of Generic structure of an FPGA fabric and explain it. **(08 Marks)**

OR

8 a. Construct a stick diagram for an multiplexer shown in Fig.Q8(a) using CMOS.

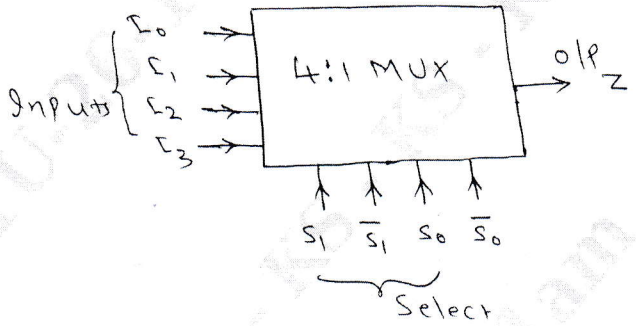

Fig.Q8(a) **(08 Marks)**

b. Explain the goals and techniques of FPGA based system design. **(08 Marks)**

Module-5

9 a. What are the requirements for system timing considerations? **(06 Marks)**

b. Explain the operation of a three transistor dynamic RAM cell. **(06 Marks)**

c. Write a note on stuck - at faults. **(04 Marks)**

OR

10 a. With the help of block diagram, explain the process of logic verification. **(08 Marks)**

b. Explain the operation of CMOS pseudo-static memory cell. **(08 Marks)**

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15EC64

Sixth Semester B.E. Degree Examination, Dec.2019/Jan.2020
Computer Communication Networks

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Mention the layers of TCP/IP protocol suite and explain briefly about layers and protocols in each layer. **(10 Marks)**

b. Define bit stuffing. Perform bit stuffing for given data 000111111100111110100 assume flag as 01111110. **(06 Marks)**

OR

2 a. Explain stop and wait protocol. **(08 Marks)**

b. (i) Define byte stuffing. **(02 Marks)**

(ii) Perform byte stuffing for frame payload in which E is the Escape byte, F is the Flag byte, and D is the data byte other than an Escape or a Flag Character.

D	E	D	D	E	D	D	E	F	D	F	D

(06 Marks)

Module-2

3 a. Explain 1-persisent, non-persistent and p-persistent methods of (CSMA) Carrier Sense Multiple Access. **(06 Marks)**

b. Explain the Ethernet frame format of standard Ethernet. **(06 Marks)**

c. In a standard Ethernet with the transmission rate of 10 Mbps, length of the medium is 2500 meters and size of the frame is 512 bits. The propagation speed of the signal in the cable is normally 2×10^8 mts/sec. Find :

(i) Propagation delay
(ii) Transmission delay
(iii) Number of frames that can fit in the medium
(iv) Efficiency **(04 Marks)**

OR

4 a. Explain working of (CSMA/CD) carrier sense multiple access/collision detection. **(08 Marks)**

b. Discuss polling as a controlled access technique. **(04 Marks)**

c. A slotted ALOHA network transmits 200 bit frames using a shared channel with a 200 Kbps bandwidth. Find the throughput if the system (all stations together) produce.

(i) 1000 frames/sec
(ii) 500 frames/sec
(iii) 250 frames/sec **(04 Marks)**

Module-3

5 a. What are the characteristics of wireless LAN? **(05 Marks)**

b. Write a note on Piconet and Scatternet in Bluetooth. **(05 Marks)**

c. Explain the characteristics of Virtual Local Area Network (VLAN) used to group stations. **(06 Marks)**

OR

6 a. Explain the following interconnecting devices:
(i) Hub
(ii) Link layer switch
(iii) Router **(06 Marks)**

b. What is NAT? Explain how NAT helps in Address depletion (Network Address Translation). **(05 Marks)**

c. Find the spanning tree and logical connection between the switch.

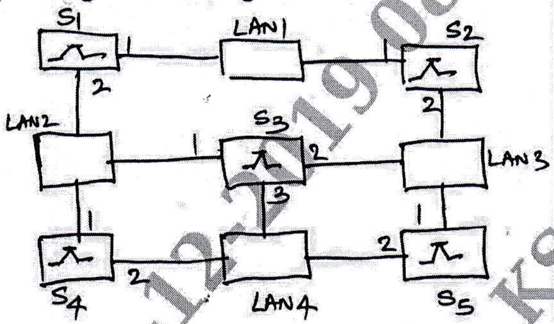

Fig.Q6(c)

S_1, S_2, S_3, S_4, S_5 are switches **(05 Marks)**

Module-4

7 a. Explain IPV4 datagram format. **(08 Marks)**

b. Explain three phases of remote host and mobile host communication. **(08 Marks)**

OR

8 a. Explain least cost tree using shared link state data base with suitable example. **(10 Marks)**

b. With a neat diagram, explain general format of ICMP messages. **(06 Marks)**

Module-5

9 a. With a neat diagram, explain connection establishment, data transfer and connection termination in Transmission Control Protocol (TCP). **(10 Marks)**

b. The following is the content of UDP (User Datagram Protocol) header in hexadecimal format CB84000D001C001C. Find:
i) What is the source port number?
ii) What is the Destination port number?
iii) What is the total length of the user datagram?
iv) What is the length of the data?
v) Is the packet directed from a client to a server or vice versa? **(06 Marks)**

OR

10 a. Briefly explain TCP segment format. **(10 Marks)**

b. Explain different field in user datagram packet format with a neat diagram. **(06 Marks)**

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15EC651

Sixth Semester B.E. Degree Examination, Dec.2019/Jan.2020
Cellular Mobile Communication

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Illustrate the concept of cellular frequency reuse with suitable schematic. **(06 Marks)**

b. Define Brewster angle. Calculate the Brewster angle, θ_B for a wave impinging on poor ground, having a permittivity of $\varepsilon_r = 4$ at the frequency of 100 MHz. Also calculate the same for typical ground with permittivity of $\varepsilon_r = 15$. **(06 Marks)**

c. Explain hata outdoor propagation model. **(04 Marks)**

OR

2 a. What are the different approaches used to expand the capacity of cellular systems? **(10 Marks)**

b. If a transmitter produces 50W of power, express the transmit power in units of (i) dBm and (ii) dBW. If 50W is applied to a unity gain antenna with 900 MHz carrier frequency, find the received power in dBM at a free space distance of 100m from the antenna. What is P_r (10 km)? Assume unity gain for the receiver antenna. **(06 Marks)**

Module-2

3 a. Explain spread spectrum channel sounding system with a neat block diagram. What are the advantages and disadvantages of the same? **(10 Marks)**

b. An urban RF radio channels are modeled on SIRCIM and SMRCIM statistical channel models with excess delays as large as 150 μs and microcellular channels with excess delays no larger than 40 μs. If the multipath bin is selected at 70. Calculate:

(i) $\Delta\tau$

(ii) The maximum bandwidth which two models can accurately represent

(iii) If the indoor channel model with excess delays as large as 500 ns exists, calculate the values of (i) and (ii) **(06 Marks)**

OR

4 a. What are the physical factors influence small scale fading in the radio propagation channel? **(08 Marks)**

b. Explain Rayleigh and Ricean Fading distribution with suitable equations. **(08 Marks)**

Module-3

5 a. With a neat diagram, explain GSM system architecture. **(06 Marks)**

b. What are the logical and physical channels associated with GSM? Explain them in detail. **(10 Marks)**

OR

6 a. Explain the location registers and security related registers associated with GSM. Mention their functions. **(06 Marks)**

b. Explain different kinds of bursts of GSM. **(10 Marks)**

Module-4

7 a. Explain the Multimedia Messaging Service Network Architecture (MMNSA) with a neat diagram. **(08 Marks)**

b. Explain the location updating procedure used in GSM. **(08 Marks)**

OR

8 a. Explain the GPRS system architecture and interfaces with a diagram. **(08 Marks)**

b. Explain the effects of Edge on the GSM system architecture. **(08 Marks)**

Module-5

9 a. Explain packet core network with suitable diagram of elements of the CDMA 2000 network. **(06 Marks)**

b. Explain the generation of the CDMA reverse access channel and reverse traffic channel with relevant schematic. **(10 Marks)**

OR

10 a. Explain CDMA mobile originated call and BS originated call with suitable time line sketch. **(08 Marks)**

b. What are the four system activities involved in a packet data session over CDMA 2000? **(08 Marks)**

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15EC663

Sixth Semester B.E. Degree Examination, Dec.2019/Jan.2020
Digital System Design Using Verilog

Time: 3 hrs. Max. Marks: 80

Note: ***Answer FIVE full questions, choosing one full question from each module.***

Module-1

1 a. Explain the following constraints imposed in real world circuits : (i) Noise margin (ii) Static levels (iii) Propagation delay (iv) Static and dynamic power consumption. **(08 Marks)**

b. Explain with illustration a simple methodology followed in IC industries. **(08 Marks)**

OR

2 a. Develop a verilog model for a 7 segment decoder. **(05 Marks)**

b. Develop a verilog model of a debouncer for a push button switch that uses a debouncer interval of 10 mS. Assume the system clock frequency is 50 MHz. **(05 Marks)**

c. Write a brief notes on finite state machine. **(06 Marks)**

Module-2

3 a. Design a 64 K * 8 bit composite memory using four 16 K × 8 bit components. **(06 Marks)**

b. Explain the different ROM's used in digital system. **(06 Marks)**

c. Compute the 12 bit ECC word corresponding to the 8-bit data word 01100001. **(04 Marks)**

OR

4 a. Explain briefly about asynchronous static RAM. **(08 Marks)**

b. Develop a verilog model of a dual port, 4K × 16bit flow through SSRAM. One port allows data to be written and read, while the other port only allows data to be read. **(05 Marks)**

c. Write a note on DRAM. **(03 Marks)**

Module-3

5 a. Explain briefly about the sequence of steps involved in IC manufacture. **(06 Marks)**

b. What are the distinguishes between a plat form FPGA from a simple FPGA? **(06 Marks)**

c. Explain the differential signaling. **(04 Marks)**

OR

6 a. Write a note on complex PLDs. **(08 Marks)**

b. Explain briefly about the internal organization of an FPGA with a neat diagram. **(08 Marks)**

Module-4

7 a. Explain the analog inputs used in input devices. **(04 Marks)**

b. Explain any four serial interface standards. **(08 Marks)**

c. Explain briefly the tristate buses and weak keepers. **(04 Marks)**

OR

8 a. Design and develop the verilog code for an input controller that has 8-bit binary coded input from a sensor. The value can be read from an 8-bit input register. The controller should interrupt the embedded Gumnut core when the input value changes. The controller is the only interrupt source in the system. **(08 Marks)**

b. Show how 64-bit data word can be transmitted serially between two ports of a system. Assume that the transmitter and the receiver are both within the same clock domain and that the signal start is set to 1 on a clock cycle in which data is ready to be transmitted. **(08 Marks)**

Module-5

9 a. Explain the hardware and software co design flow. **(08 Marks)**

b. Explain the design optimization that are must to meet the design constraints. **(08 Marks)**

OR

10 Write a short notes on :

a. Scan design and boundary scan. **(08 Marks)**

b. Built-In Self Test (BIST) **(08 Marks)**

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15TE63

Sixth Semester B.E. Degree Examination, Dec.2019/Jan.2020
Microwave Theory and Antennas

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Describe the operation of the reflex klystron oscillator with the aid of suitable diagram. **(08 Marks)**

b. A certain transmission line has a characteristic impedance of 75 + j0.01Ω and it is terminated in a load impedance of 70 + j50Ω. Compute:
i) The reflection co-efficient
ii) The transmission coefficient
iii) Show that transmission coefficient equals the algebraic sum of 1 plus the reflection coefficient. **(08 Marks)**

OR

2 a. A lossless line of characteristic impedance R_o = 50Ω is to be matched to a load $Z_l = \left[\frac{50}{2 + j(2+\sqrt{3})}\right]^{\Omega}$ by means of a short circuited stub. The characteristic impedance of the stub is 100Ω. Find the stub position and length of the stub so that a match is obtained. **(08 Marks)**

b. A reflux Klystron is to be operated at a frequency of 10GHz with the following specifications:
D.C. beam voltage = 300V
Repeller space = 0.1cm
Mode = $1\frac{3}{4}$ mode.
Calculate: i) P_{RFmax} ii) Repeller voltage for a beam current of 20mA. **(04 Marks)**

c. List the applications of the Smith Chart. **(04 Marks)**

Module-2

3 a. Prove that impedance matrices are symmetrical for a reciprocal microwave junction. **(08 Marks)**

b. Define the terms directivity and directional coupling as used with directional coupler and explain their significance. **(08 Marks)**

OR

4 a. Define insertion loss, return loss for multiport networks. **(06 Marks)**

b. Explain the operation of Faraday rotation ferrite isolator. **(06 Marks)**

c. What are the applications of magic-Tee in microwave networks? **(04 Marks)**

Module-3

5 a. Define: Radiation intensity, effective height of an antenna. **(08 Marks)**

b. A lossless parallel strip line has a conducting strip width W. The substrate dielectric separating the two conducting strips has a relative dielectric constant $\in_{rd}$ of 6 and a thickness of 4mm (d). Calculate:

i) The required width w of the conducting strip in order to have a characteristic impedance of 50Ω.

ii) The strip line capacitance

iii) The strip line inductance

iv) The phase velocity of the wave in parallel strip line. **(08 Marks)**

OR

6 a. Show that the effective height and effective aperature are related via radiation resistance and intrinsic impedance of space. **(08 Marks)**

b. A coplanar strip line carries an average power of 250mw and peak current of 100mA. Determine the characteristic impedance of the coplanar strip line. **(04 Marks)**

c. Define: HPBW of an antenna. **(04 Marks)**

Module-4

7 a. Obtain the expression for field pattern E of two isotropic point sources of equal amplitude and same phase. Assume two sources are separated by λ/2. Plot the pattern. **(08 Marks)**

b. A source has a sine squarrel radiation intensity power pattern. Find its directivity. **(04 Marks)**

c. Obtain the pattern factor for the full wave thin linear antenna. **(04 Marks)**

OR

8 a. Obtain the expression for radiation resistance of a short electric dipole. **(08 Marks)**

b. Obtain the total field expression at a large distance for linear arrays of 'n' isotropic-point sources of equal amplitude and spacing. **(08 Marks)**

Module-5

9 a. Derive an expression for the instantaneous electric field E_θ at a large distance 'r' from a loop antenna of radius 'a'. **(10 Marks)**

b. A 16-turn helical beam antenna has a circumference of λ and turn spacing of λ/4 what is i) HPBW ii) axial ratio iii) Power pattern. **(06 Marks)**

OR

10 a. With the aid of appropriate sketches, explain Horn antenna design considerations. **(08 Marks)**

b. With the aid of neat diagram, describe the design considerations of log-periodic antenna. What are the applications of log-periodic antenna array? **(08 Marks)**

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