USN | | | | | | | | | | |

10EC/TE71

Seventh Semester B.E. Degree Examination, Dec.2018/Jan.2019
Computer Communication Networks

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

PART – A

1 a. Describe ISO-OSI reference model of computer network. Discuss the function of each layer. **(10 Marks)**

b. Explain the operation of ADSL using multitone modulation with a neat diagram. **(06 Marks)**

c. List different types of addressing in TCP/IP. Explain any one type of addressing with suitable example. **(04 Marks)**

2 a. What is framing? Explain bit and character stuffing with help of example. **(06 Marks)**

b. Explain different types of HDLC frames. **(06 Marks)**

c. Explain design of stop and wait automatic repeat frames for a noisy channel. **(08 Marks)**

3 a. With a flow diagram, explain 1-persistent, P-Persistent and non-persistent MAC procedures. **(06 Marks)**

b. Discuss with an example CDMA channelization protocol. **(08 Marks)**

c. Explain Token passing controlled access technique. **(06 Marks)**

4 a. Explain IEEE802.3 MAC frame format. **(06 Marks)**

b. Compare and contrast standard, fast and Gigabit Ethernet. **(06 Marks)**

c. Explain in detail IEEE 802.11 MAC protocol. **(08 Marks)**

PART – B

5 a. Discuss different inter connecting devices on the basis of the layers they operate. **(08 Marks)**

b. Explain bus back bone and star back bone networks. **(04 Marks)**

c. What are virtual LAN's? What is the basis for membership in VLAN? Enumerate advantages of having VLAN's. **(08 Marks)**

6 a. Compare between IPV4 and IPV6 packet headers along with extension headers. **(08 Marks)**

b. Discuss three strategies proposed by IETF to help the transition between IPV4 and IPV6. **(08 Marks)**

c. Write short notes on logical addressing. **(04 Marks)**

7 Write short notes:

(i) Forwarding techniques.

(ii) Routing Information Protocol.(RIP)

(iii) Border Gateway Protocol (BGP).

(iv) Multicasting distance vector routing protocol (DVMRP) **(20 Marks)**

8 a. Explain TCP and UDP datagram. **(12 Marks)**

b. Describe TCP connection establishment using three way handshakes. **(08 Marks)**

* * * * *

USN | | | | | | | | | | |

10EC/TE72

Seventh Semester B.E. Degree Examination, Dec.2018/Jan.2019

Optical Fiber Communication

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Draw and explain the detailed block diagram of optical fiber communication system over other general type of communication system. List its advantages and disadvantages. **(10 Marks)**

b. What is numerical aperture and acceptance angle? Derive an expression for numerical aperture and maximum acceptance angle in the case of a step index optical fiber in terms of refractive indices of core and cladding material. **(06 Marks)**

c. Calculate the number of modes at 850 nm and 1.2 μm in a GRIN fibre with a parabolic-index profile, $\alpha = 2$, with core radius = 25 μm, $n_1 = 1.5$ and $n_2 = 1.49$. **(04 Marks)**

2 a. Discuss the importance of signal attenuation. Explain the three main mechanisms which cause absorption loss of optical energy in fiber. **(08 Marks)**

b. A continuous 12 km long optical fiber link has a loss of 1.5 dB/km.
i) What is the minimum optical power level that must be launched into the fiber to maintain as optical power level of 0.3 μW at the receiving end?
ii) What is the required input power if the fiber has a loss of 2.5 dB/km? **(04 Marks)**

c. Explain the various types of chromatic dispersion which results from the finite spectral line width of the optical source. **(08 Marks)**

3 a. Derive the expression for internally generated power and efficiency in a LED. **(08 Marks)**

b. Give the comparison between PIN diode and APD considering the different parameters. **(06 Marks)**

c. A planar LED is fabricated from gallium arsenide which has a refractive index of 3.6.
i) Calculate the optical power emitted into air as a percentage of the internal optical power for the device when the transmission factor at the crystal-air interface is 0.68.
ii) When the optical power generated internally is 50% of the electric power supplied, determine the external power efficiency. **(06 Marks)**

4 a. Define Fiber Optic Splice. With the help of neat diagram, explain any two types of splicing techniques. **(07 Marks)**

b. List and explain the principle requirements of a good connector design. **(04 Marks)**

c. Explain the concepts of mechanical misalignment, fiber related losses and fiber-end-face preparation with respect to fiber-to-fiber joints. **(09 Marks)**

PART – B

5 a. Explain with help of neat diagram, how the eye diagram is powerful measurement tool for assessing data handling ability in a digital transmission system. **(10 Marks)**

b. Describe the working principles of Burst Mode Receiver and Analog Receiver. **(10 Marks)**

6 a. What is rise time budget? Derive an expression for total system rise time budget. **(10 Marks)**
b. Explain mode-partition noise and chirping. **(10 Marks)**

7 a. With the help of a neat schematic diagram, explain the operational principle of WDM system with multiplication in capacity of system. **(10 Marks)**
b. Describe the working of Dynamic Gain Equaliser and Optical add/drop Multiplexers (OADM). **(10 Marks)**

8 a. List the three possible configurations of an EDFA. With relevant diagram explain any one of them. Also derive an expression for EDFA power conversion efficiency and gain. **(10 Marks)**
b. With relevant diagrams, explain the basic formats of an STS-N SONET frame, STM-N SDH frame, two fiber UPSR and four fiber BLSR. **(10 Marks)**

* * * * *

USN | | | | | | | | | | |

10EC73

Seventh Semester B.E. Degree Examination, Dec.2018/Jan.2019

Power Electronics

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Sketch control characteristics of the following:
i) Thyristor switch ii) GTO switch
iii) BJT switch iv) MOSFET switch **(08 Marks)**

b. Explain briefly the following power electronic circuits:
i) AC-DC controlled rectifier ii) AC voltage controller
iii) DC chopper iv) Inverters **(08 Marks)**

c. Explain peripheral effect with respect to power converters. **(04 Marks)**

2 a. Draw the switching model of MOSFET and explain its switching characteristics. **(08 Marks)**

b. The beta (β) of bipolar transistor shown in Fig.Q2(b) varies from 12 to 75. The load resistance R_C = 1.5 Ω. The dc supply voltage V_{CC} = 40 V and the input voltage to the base circuit V_B = 6V, if $V_{CB(sat)}$ = 1.6V, $V_{CE(sat)}$ = 1.2 V, R_B = 0.7 Ω. Determine:
i) Over drive factor ii) Forced β iii) Power loss in transistor.

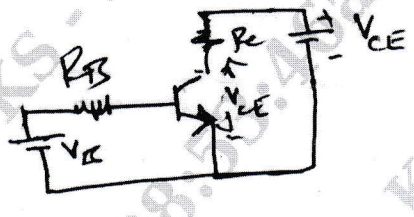

Fig.Q2(b) **(08 Marks)**

c. Sketch the symbol and circuit of IGBT as switch. Mention important features of IGBT. **(04 Marks)**

3 a. Explain two-transistor model of thyristor and hence derive anode current equation in terms of gate current, gain and leakage current. **(08 Marks)**

b. Draw and explain synchronized UJT relaxation oscillator circuit for turning on of SCR. **(08 Marks)**

c. The thyristor in the circuit shown in Fig.Q3(c) has a latching current of 50 mA and is triggered by pulse width of 50 μS. Show without R′, thyristor will fail to remain ON. Calculate R′ to ensure firing of thyristor.

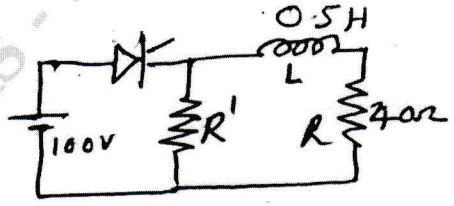

Fig.Q3(c) **(04 Marks)**

4 a. With circuit diagram and waveforms explain the working of 1-ϕ-full converter with RLE load. **(08 Marks)**

b. With neat circuit diagram and waveform explain the working of 1-ϕ dual converter. **(08 Marks)**

c. The single phase dual converter is operated from a 120V, 60 Hz supply and the load resistance is R = 10 Ω. The circulating inductance is L_r = 40 mH; delay angle $\alpha_1 = 60°$ and $\alpha_2 = 120°$. Calculate the peak circulating current and the peak current of converter 1. **(04 Marks)**

PART – B

5 a. Explain the working of impulse commutation with neat circuit and waveforms. **(08 Marks)**

b. In the circuit of Fig.Q5(b) shown the capacitor is initially charged to a voltage of $V_C(0)$ = -500 V. If L = 15 μH and C = 50 μF and the SCR is turned on at t = 0. Calculate Peak value of resonant current and the conduction time of thyristor.

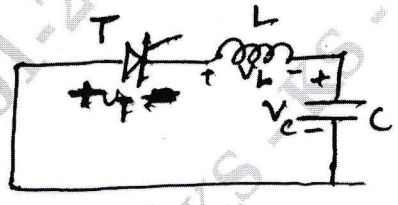

Fig.Q5(b) **(08 Marks)**

c. Explain external pulse commutation with neat circuit diagram. **(04 Marks)**

6 a. Explain the working of ON-OFF type AC voltage controller. Derive expression for RMS output voltage. **(08 Marks)**

b. Explain with neat sketch and waveforms, single phase AC voltage controller with RL load. Derive expression for V_{orms}. **(08 Marks)**

c. A single phase full wave ac voltage controller has a resistive load of R = 10 Ω and the input voltage is V_s = 120 V, 60 Hz. The delay angles of thyristors T_1 and T_2 are equal $\alpha_1 = \alpha_2 = \alpha = \pi/2$. Determine: i) V_{orms} ii) input PF iii) the average current of thyristors, I_A iv) the rms thyristor current, I_A **(04 Marks)**

7 a. Explain the working of class E chopper. Also explain the working principle of step-down chopper and derive expression for:
i) Average output voltage
ii) Output power **(08 Marks)**

b. Explain the working principle of step-up chopper with neat circuit diagram and waveform. Derive expression for average output voltage. **(08 Marks)**

c. A step-down chopper is operation at a frequency of 2 kHz from a 250 V dc source to supply a load resistance of 10 Ω. The time constant of the load circuit is 10 ms. If the average load voltage is 150 V, calculate: i) On-time of the chopper ii) the average and rms values of load current, iii) peak-to-peak ripple current. **(04 Marks)**

8 a. With neat circuit and waveforms, explain the working of 1-ϕ-full bridge inverter. Define the performance parameters related to the inverter. **(08 Marks)**

b. Explain the working of transistorized 1-ϕ-current source inverter with neat circuit diagram and waveforms. **(08 Marks)**

c. The single phase bridge inverter has source voltage of 60 V and R = 5 Ω. Calculate: i) rms output voltage at fundamental frequency ii) rms output power iii) total harmonic distortion iv) distortion factor **(04 Marks)**

* * * * *

USN | | | | | | | | | | |

10EC74

Seventh Semester B.E. Degree Examination, Dec.2018/Jan.2019
Embedded System Design

Time: 3 hrs. Max. Marks:100

Note: *Answer any FIVE full questions, selecting atleast TWO questions from each part.*

PART – A

1 a. Define :
(i) An embedded system
(ii) Soft Real time system
(iii) Watch Dog Timer **(06 Marks)**

b. Explain a microprocessor based embedded system with the help of a neat diagram. **(06 Marks)**

c. Sketch the embedded system lifecycle and explain the various stages involved in it. **(08 Marks)**

2 a. Explain indexed mode and register indirect addressing modes with diagrams. Also write the timing diagram for serial write operation with a 8-bit register. **(08 Marks)**

b. With a neat block diagram, explain the architecture of the datapath and the memory interface for a simple microprocessor at RTL. **(06 Marks)**

c. Compare :
(i) Big Endian and Little Endian formats
(ii) RISC and CISC registers
(iii) Truncation and Rounding errors. **(06 Marks)**

3 a. Design a 4K×16 SRAM system and explain briefly. **(08 Marks)**

b. Write the inside and outside diagrams for DRAM along with read operation. **(06 Marks)**

c. Explain associative mapping cache implementation. **(06 Marks)**

4 a. Briefly explain waterfall, V cycle and spiral life cycle models with neat flow diagrams. **(10 Marks)**

b. Write a hardware architecture and data and control flow diagram of a counter system and explain the flow diagram briefly. **(06 Marks)**

c. Discuss functional model versus architectural models of an Embedded system. **(04 Marks)**

PART – B

5 a. Differentiate between :
(i) Program and process
(ii) Processes and threads
(iii) Supervisor and user privilege modes **(06 Marks)**

b. Explain any 6 functions of an embedded operating system? **(06 Marks)**

c. Discuss Task control block with a neat diagram. Explain the major components involved in TCB. **(06 Marks)**

d. Draw the Task state diagram. **(02 Marks)**

6 a. What is foreground and background systems? Write the differences between foreground and background tasks. (05 Marks)
b. Describe virtual model and high level model for operating system architecture. (05 Marks)
c. Write the algorithm for a simple OS kernel, using C language notation for 3 asynchronous tasks using TCBs only. The 3 tasks use a common data buffer for read, increment and display operations. (08 Marks)
d. Mention four categories of multitasking OS? (02 Marks)

7 a. Write the Amdahl's limitation for performance / optimization. Consider system with the following characteristics. The task to be analysed and improved currently executes in 100 time units, and the goal is to reduce execution time to 80 time units. The algorithm to be improved uses 40 time units. Determine the unknown parameter and write the inference. (06 Marks)
b. Write C function to determine the sum of the elements in an array and analyse it for its time complexity. (06 Marks)
c. Explain the Big-O notation used for comparing the algorithms along with table and graphs. Mention the rules used for Big-O arithmetic. (08 Marks)

8 a. Write short notes on the following :
(i) Tricks of the trade
(ii) Performance Optimization (10 Marks)
b. Write and analyse a linear search algorithm for its time complexity. (05 Marks)
c. Describe memory loading with equation and an example. (05 Marks)

* * * * *

USN | | | | | | | | | | |

10EC751

Seventh Semester B.E. Degree Examination, Dec.2018/Jan.2019
DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Briefly explain the digital signal processing system. **(06 Marks)**

b. Briefly explain the FIR filter. **(08 Marks)**

c. Explain discrete time sequence in detail. **(06 Marks)**

2 a. Briefly explain the Parallel Multiplier. **(06 Marks)**

b. Briefly explain the Barrel shifter. **(06 Marks)**

c. Discuss the following indirect addressing modes:
(i) Post_increment (ii) Pre_Subtract_offset
(iii) Pre_decrement (iv) Post_add_offset **(08 Marks)**

3 a. Briefly explain the functional diagram of the central processing unit of TMS320C54XX processor. **(06 Marks)**

b. Briefly explain the block diagram of circular addressing modes of TMS320C54XX processor **(06 Marks)**

c. Assuming the current contents of AR_3 to be 200h, what will be its contents after each of the following TMS320C54XX addressing modes is used? Assume that the contents of AR_0 are 20h.
(i) $*AR_3+0$ (ii) $*AR_3+$ (iii) $*+AR_3(40h)$ (iv) $*+AR_3(-40h)$ **(08 Marks)**

4 a. Show the pipeline operation of the following sequence of instructions if the initial values of AR_1, AR_3, A are 84, 81, 1 and the values stored in memory location 81, 82, 83, 84 are 2, 3, 4, 6. Also provide the values of registers AR_3, AR_1, T and accumulator A after completion of each cycle.

```
ADD *AR3+, A
LD *AR1+, T
MPY *AR3+, B
ADD B, A
```

(08 Marks)

b. Write the program to compute multiply and accumulate using direct addressing mode
$y(n) = h(0)\,x(n) + h(1)\,x(n-1) + h(2)\,x(n-2)$ **(06 Marks)**

c. Briefly explain the Host Port Interface (HPI) with important signals. **(06 Marks)**

PART – B

5 a. What are the values are represented by the 16-bit fixed point number N = 4000h in Q_{15} and Q_7 Notation. **(02 Marks)**

b. Write a program for Digital interpolation using a FIR filter with interpolation factor = 5 for TMS320C54XX processor. **(10 Marks)**

c. Write an Assembly Language Program for second_order IIR filter using TMS320C54XX. **(08 Marks)**

6 a. Derive the optimum overflow and scaling in DIT-FFT algorithm. **(06 Marks)**
b. Write a program for signal spectrum in DIT-FFT Algorithm using TMS320C54XX. **(06 Marks)**
c. Write a program for Butterfly computation in DIT-FFT Algorithm using TMS320C54XX. **(08 Marks)**

7 a. Briefly explain Handling of interrupts in TMS320C54XX processor. **(06 Marks)**
b. Briefly explain the programmed I/O in TMS320C54XX processor. **(08 Marks)**
c. Briefly explain the Register subaddressing technique for configuration DMA operation. **(06 Marks)**

8 a. Briefly explain Synchronous Serial Interface (SSI). **(06 Marks)**
b. Briefly explain clipping autocorrelation pitch detector. **(06 Marks)**
c. Briefly explain JPEG Encoder and JPEG Decoder. **(08 Marks)**

* * * * *

USN | | | | | | | | | | |

10EC755

Seventh Semester B.E. Degree Examination, Dec.2018/Jan.2019
Applied Embedded System Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Explain the process of converting assembly language program to machine code and finally obtain ROM image. **(10 Marks)**

b. Discuss the design process in embedded system. **(10 Marks)**

2 a. Explain the various types of instructions in 8051 instruction set. **(08 Marks)**

b. Discuss Princeton and Harvard architecture. **(06 Marks)**

c. Explain ARM7 registers and 3–stage pipeline architecture. **(06 Marks)**

3 a. List the features of sophisticated interfacing device ports. **(08 Marks)**

b. Explain the following serial communication ports :
i) SPI ii) SCI iii) SI. **(12 Marks)**

4 a. Explain DMA with a diagram. **(10 Marks)**

b. Explain the classification and sources of interrupts. **(10 Marks)**

PART – B

5 a. Highlight the advantages of assembly and high level languages. **(10 Marks)**

b. Explain :
i) Source files
ii) Configuration files
iii) Preprocessor directives
iv) Pointers
v) Macros. **(10 Marks)**

6 a. Explain the UML Basic elements. **(10 Marks)**

b. Discuss various program models. **(10 Marks)**

7 a. Explain features of message queue. **(05 Marks)**

b. Write short notes on :
i) Semaphore functions
ii) Pipe functions
iii) RPC functions. **(15 Marks)**

8 a. Define RTOS. Explain RTOS facilities. **(10 Marks)**

b. List and explain memory saving strategy for a system. **(10 Marks)**

* * * * *

USN | | | | | | | | | | |

10EC763

Seventh Semester B.E. Degree Examination, Dec.2018/Jan. 2019
Image Processing

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. What are the fundamental steps of digital image processing? **(12 Marks)**
b. Explain brightness adaptation and discrimination. **(08 Marks)**

2 a. Explain image acquisition using single sensor and senor strips with necessary diagrams. **(12 Marks)**
b. What do you understand by image sampling and quantization? **(08 Marks)**

3 a. Mention 2-dimensional orthogonal transform for an image. **(05 Marks)**
b. Define separable unitary transforms. **(05 Marks)**
c. Explain 5-properties of 2-D DFT. **(10 Marks)**

4 a. Define 2-D forward and inverse discrete sine transform and mention its properties. **(10 Marks)**
b. Generate (4 × 4) slant transform matrix given the core matrix $s_1 = \frac{1}{\sqrt{2}}\begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix}$. Also mention its properties. **(10 Marks)**

PART – B

5 a. What do you mean by image enhancement? Explain 3 types of basic intensity level transformations. **(10 Marks)**
b. A 3 bit image of size 64 × 64 has intensity distribution as shown in table. Implement histogram equalization and plot the same. **(10 Marks)**

Gray level	0	1	2	3	4	5	6	7
Number of pixels	790	1023	850	656	329	245	122	81

Table Q5(b)

6 a. With necessary block diagram. Explain fundamental steps used in frequency domain enhancement. **(08 Marks)**
b. Briefly explain homomorphic filtering and its implementation. **(12 Marks)**

7 a. Differentiate between image restoration and image enhancement. Briefly explain the image degradation model. **(10 Marks)**
b. With necessary mathematical equation, explain different noise model. How will you remove the noise in an image? **(10 Marks)**

8 a. Describe the RGB color model. How their color can be converted to HSI color model? **(10 Marks)**
b. What is pseudo color image processing? How does a gray image covert into color image? **(10 Marks)**

* * * * *

USN | | | | | | | | | | |

10TE73

Seventh Semester B.E. Degree Examination, Dec.2018/Jan.2019
Wireless Communication

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO full questions from each part.***

PART – A

1 a. Discuss the general history and evolution of wireless technology. **(10 Marks)**

b. Explain the characteristics of 2G and 3G cellular systems. **(10 Marks)**

2 a. With a neat block diagram, explain common cellular system components. **(10 Marks)**

b. Explain a mobile terminated call in a cellular network with a neat flow diagram. **(10 Marks)**

3 a. Explain briefly the following capacity expansion techniques i) Cell splitting ii) Cell sectoring iii) Overlaid cells. **(12 Marks)**

b. Explain different functions of mobility management. **(08 Marks)**

4 a. List the various logical channels used in GSM. **(10 Marks)**

b. Explain TDMA concept and how it is implemented in GSM. **(10 Marks)**

PART – B

5 a. List different call setup operation in GSM system. Explain any two operations in detail. **(10 Marks)**

b. Explain GSM inter BSC hand over operation with necessary diagram. **(10 Marks)**

6 a. Explain the process of soft hand off in CDMA. **(10 Marks)**

b. Explain the following terms:
i) Synchronization channel
ii) Pilot channel. **(10 Marks)**

7 a. Explain various digital modulation techniques used in wireless communication. **(10 Marks)**

b. Explain Error Detection and correction toding technique used in wireless communication. **(10 Marks)**

8 a. Explain with a neat block diagram, the function of RAKE receiver. **(10 Marks)**

b. Explain the Bluetooth protocol stack with relevant figures. **(10 Marks)**

* * * * *

USN | | | | | | | | | | |

10TE74

Seventh Semester B.E. Degree Examination, Dec.2018/Jan.2019
DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. With a neat block diagram, explain the scheme of a DSP system. **(06 Marks)**

b. Explain in brief the issues to be considered in designing and implementing a DSP system. **(06 Marks)**

c. Explain the two methods of sampling rate conversions used in DSP, with suitable block diagrams and examples. **(08 Marks)**

2 a. What is a barrel shifter in a DSP device and why it is used? Explain how a 4 – bit shift right barrel shifter can be complemented. **(06 Marks)**

b. Draw the MAC unit used in DSP. Explain any two methods used to avoid overflow and underflow. **(08 Marks)**

c. DSP has a circular buffer with start and end addresses as 0200 h and 0310 h respectively. What is the buffer size? What would be the new values of the address pointer of the buffer, if in course of address computation gets updated to i) 0366 h ii) 0192 h. **(06 Marks)**

3 a. With the help of functional diagram, explain about multiplier / adder unit of TMS320C54XX processor. **(06 Marks)**

b. With a block diagram, explain the indirect addressing mode of TMS320C54XX processor using dual memory operand. **(06 Marks)**

c. Assume that the register AR_4 with contents 2040h is selected as the pointer for circular buffer. Let B_k = 50h. Determine start and end addresses for the buffer. What will be the content of register AR_4 after the execution of the instruction? **(08 Marks)**
i) LD * AR_4 + 0 % , A ii) LD * AR_4 – OB, A , if the contents of AR_0 is 0035h.

4 a. Briefly explain the following instruction of 54XX processor , **(08 Marks)**
i) MPY * AR_3- , * AR_4 + 0 , B ii) ADD * AR_2 + , 6, A
iii) MAC * AR_5 + , # 1234, B iv) RPT # K.

b. Write a short note on Host Port Interface. **(06 Marks)**

c. By means of a figure, explain the pipeline operation of the following sequences of instruction , if the initial values of AR_1, AR_3 , A are 104, 101, 2 and the values stored in the memory locations 101, 102, 103, 104 are 4, 6, 8, 12. Also provide the values of registers AR_3, AR_1, T and accumulator A, after completion of each cycle.
ADD * AR_3 + , A
LD * AR_1 + , T
MPY * AR_3 + B
ADD B, A. **(06 Marks)**

PART – B

5 a. What are the values represented by a 16 – bit number N = 5736h in Q_0, Q_6, Q_{10} and Q_{15} notation. **(08 Marks)**

b. Write a TMS320C54XX program that illustrate the multiplication of two Q_{15} numbers to produce a Q_{15} result. **(06 Marks)**

c. Write the schematic and explain the memory organization for implementation of an FIR filter of order N. **(06 Marks)**

6 a. Determine the following for a 512 point FFT computation :
i) Number of stages ii) Number of butterflies in each stage.
iii) Number of butterflies needed for entire computation.
iv) Number of butterflies that need no twiddle factor.
v) Number of butterflies that need real twiddle factor.
vi) Number of butterflies that need complex twiddle factor. **(06 Marks)**

b. Explain bit reversed address mechanism and give its implementation scheme using TMS320C54XX DSP. **(06 Marks)**

c. Explain how overflow is handled with scaling in computation of DFT. **(08 Marks)**

7 a. With the help of block diagram, explain the memory interface for TMS320C5416 processor. Also draw the timing diagram for a read – read – write sequence of operation. **(10 Marks)**

b. Design a circuit to interface a 4K × 16 and 2K × 16 memory chip to realize program memory space for the TMS320C54XX processor in the address ranges :
03FFFFh – 03F000h and 05F800h – 05FFFFh respectively. **(10 Marks)**

8 a. Explain with block diagram, the biotelemetry receiver implementation. **(06 Marks)**

b. Explain with a neat diagram, the operation of the pitch detector. **(08 Marks)**

c. Explain with a neat block diagram, the synchronous serial interface between the C54XX and a CODEC device. **(06 Marks)**

*****

USN | | | | | | | | | | |

10TE754

Seventh Semester B.E. Degree Examination, Dec.2018/Jan.2019
Image Processing

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Discuss applications of image processing. **(05 Marks)**

b. How is image formed in the eye? Explain the importance of brightness adaptation and discrimination in image processing. **(10 Marks)**

c. Explain: i) False contouring ii) Checker board pattern **(05 Marks)**

2 a. Explain the following terms:
i) Adjacency ii) Connectivity
iii) Gray level resolution iv) Spatial resolution **(08 Marks)**

b. Explain image sensing and acquisition methods. **(08 Marks)**

c. Find the time required in seconds for transmitting a monochrome image of size 2.5 " × 2" scanned at 150 DPI and to be sent at 28 KBPS speed. **(04 Marks)**

3 a. Explain properties of unitary transforms. **(04 Marks)**

b. Define 2D-discrete Fourier transform. Compute DFT matrix 'F' for N = 4. Discuss its properties. **(08 Marks)**

c. $A = \frac{1}{2}\begin{pmatrix} \sqrt{3} & 1 \\ -1 & \sqrt{3} \end{pmatrix}$ $U = \begin{pmatrix} 1 & 2 \\ 1 & 2 \end{pmatrix}$. Calculate the transformed image V and basis images. **(08 Marks)**

4 a. Explain Hadamard Transform with its properties. Compute Hadamard transform of 2 × 2 image $F = \begin{bmatrix} 3 & -1 \\ 6 & 2 \end{bmatrix}$. **(10 Marks)**

b. Define 2D-discrete Cosine transform and its inverse transform. Compute DCT matrix for N = 4. Discuss its properties. **(10 Marks)**

PART – B

5 a. Explain the use of arithmetic and logical operations for image enhancement. **(06 Marks)**

b. Using 2nd derivative, develop a Laplacian mask for image enhancement. **(08 Marks)**

c. The histogram of 8 level image of size 64 × 64 is shown in Fig.Q5(c). Perform histogram equalization and draw the histogram of equalized image.

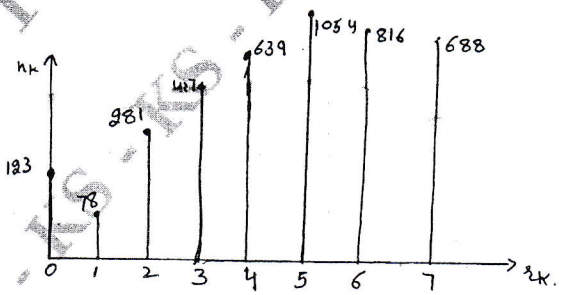

Fig.Q5(c) **(06 Marks)**

6 a. Explain homomorphic filters for image enhancement. (10 Marks)
b. Explain smoothing and sharpening filters in frequency domain. (10 Marks)

7 a. Define the process of image restoration. Explain four important noise probability density functions. (10 Marks)
b. Explain Wiener filter and inverse filtering in image processing. (10 Marks)

8 a. Convert RGB to HSI color model. (08 Marks)
b. What is pseudo color image processing? (04 Marks)
c. Explain HSI color model and its applications. (08 Marks)

* * * * *

USN | | | | | | | | | | |

10TE765

Seventh Semester B.E. Degree Examination, Dec.2018/Jan.2019
Embedded System Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO full questions from each part.***

PART – A

1 a. Explain the major elements of an embedded system design and development process including system life cycle. **(08 Marks)**

b. With a block diagram, explain microprocessor based embedded system. **(08 Marks)**

c. Explain: i) instruction cycle ii) Watch dog timer iii) Hard RTS iv) Firm RTS. **(04 Marks)**

2 a. Discuss about truncation error and rounding errors. **(06 Marks)**

b. Explain data transfer instructions with neat diagrams. **(08 Marks)**

c. Explain RTN model for a microprocessor data path and memory interface. **(06 Marks)**

3 a. With diagram explain the operation of SRAM with timing operations for read and write. **(08 Marks)**

b. Explain refresh arbitration circuit with a neat diagram. **(06 Marks)**

c. With a neat diagram, explain direct and associative mapping scheme cache implementation. **(06 Marks)**

4 a. With diagram explain: i) Water fall model ii) Spiral model. **(06 Marks)**

b. Compare functional model and architectural model. **(06 Marks)**

c. Write the hardware architecture and data, control flow diagram of a counter system and explain briefly the flow diagram. **(08 Marks)**

PART – B

5 a. Compare single thread vs multithread process with neat diagram. **(06 Marks)**

b. Explain about memory resource management and process level management. **(06 Marks)**

c. Explain the following:
i) Reentrant code
ii) Foreground and background systems
iii) Lightweight and heavy weight thread
iv) Context switch. **(08 Marks)**

6 a. Explain the functions of an embedded operating system. **(08 Marks)**

b. With a diagram, explain the structure of TCB. **(06 Marks)**

c. Explain about run time stack and application stack. **(06 Marks)**

7 a. Write the amdahls limitations for performance improvement optimizations. **(06 Marks)**

b. Explain the Big-O-Notation and Big-O-arithmatic operations. **(06 Marks)**

c. Explain array and linked list data structure. **(08 Marks)**

8 a. Explain memory loading with suitable example. **(08 Marks)**

b. Explain hardware accelerators for performance improvement. **(06 Marks)**

c. Explain the following: i) Polled loops ii) Co-routine. **(06 Marks)**

* * * * *