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10ES42

Fourth Semester B.E. Degree Examination, Dec.2016/Jan.2017
Microcontrollers

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Distinguish Harvard and Von-Neumann (Princeton) architectures with diagrams. **(06 Marks)**

b. Explain with block diagram the architectural feature of 8051 and list out salient features of 8051 microcontroller. **(08 Marks)**

c. Discuss the need for stack memory in microcontrollers. Explain with examples the PUSH and POP instructions. **(06 Marks)**

2 a. What are the addressing modes supported by 8051 μC? Explain with examples. **(08 Marks)**

b. Explain the different types of conditional and unconditional jump instructions of 8051. Specify the different ranges associated with jump instructions. **(08 Marks)**

c. Differentiate between the following instructions:
i) SWAP and XCH ii) SJMP and LJMP. **(04 Marks)**

3 a. Write a ALP to copy the most significant nibble of A in both nibbles of RAM address 3Ch. Also write the algorithm for example if A = 36h, then 3Ch = 33h. **(06 Marks)**

b. Write an ALP to add the unsigned numbers found in internal RAM locations 25h, 26h and 27h together and put the result in RAM locations 31L (MSB) and 30h (LSB). **(08 Marks)**

c. For a machine cycle of 1.085 μsec find the time delay in the following subroutine:

```
DELAY: MOV R2, # 200
AGAIN: MOV R3, # 250
HERE: NOP
      NOP
      DJNZ R3, HERE
      DJNZ R2, AGAIN
      RET.
```

(06 Marks)

4 a. With a relevant figure write a sequence of events that occur in 8051 microcontroller when the CALL and RET instructions are executed. **(06 Marks)**

b. What are the ways to create time delay? Discuss the factors affecting the accuracy of the time delay. **(07 Marks)**

c. What are the differences between timer and counter? Explain with the formats of the SFR. **(07 Marks)**

PART – B

5 a. In what way timer/counter mode 2 programming is different from mode 0 and mode 1? **(06 Marks)**

b. Write an ALP to generate square wave on pin 3.4 of ON Time 4 msec and OFF Time 3 msec, using timer 0, mode 0. Assume that crystal frequency of 8051 is 11.0592 Hz. **(08 Marks)**

c. Explain the importance of interrupt priority (IP) SFR and the beginning fixed address of the interrupt handler subroutines. **(06 Marks)**

6 a. Write the steps required for programming 8051 to transfer data serially and what is the role of PCON register in serial communication? **(07 Marks)**

b. Write a C program to interface 8051 to LCD. Draw the hardware schematic. **(07 Marks)**

c. Write a 'ALP' program to interface stepper motor to 8051, with a neat diagram of 8051 connection to stepper motor. **(06 Marks)**

7 a. Tabulate the different data types in 'C', bits and the data range. **(05 Marks)**

b. Write an 8051 C program to send two different strings to the serial port. Assuming that SW is connected to pin P2.0, monitor its status and make a decision as follows:
SW = 0, send your first name
SW = 1, send your last name.
Assume XTAL = 11.0592 MHz, baud rate of 9600, 8 bit data 1 stop bit. **(10 Marks)**

c. Write a 'C' program to serially transmit the message "HELLO" continuously at baud rate of 9600, 8-bit data and 1 stop bit. **(05 Marks)**

8 a. Briefly discuss the features of MSP 430 microcontrollers. **(06 Marks)**

b. Explain different addressing modes of MSP 430 with examples. **(08 Marks)**

c. Write a MSP 430 assembly program to find the largest in the given array of 'n' bytes. **(06 Marks)**

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10ES43

Fourth Semester B.E. Degree Examination, Dec.2016/Jan.2017
Control Systems

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. A mechanical system is shown in the Fig.Q.1(a).
i) Obtain the performance equations.
ii) Draw the electrical analog based on force-current analogy. **(08 Marks)**

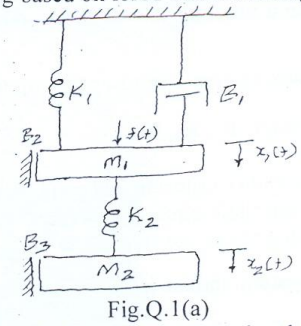

Fig.Q.1(a)

b. For the mechanical system shown in Fig.Q.1(b), draw the electrical network based on torque current analogy. Write the performance equations. **(08 Marks)**

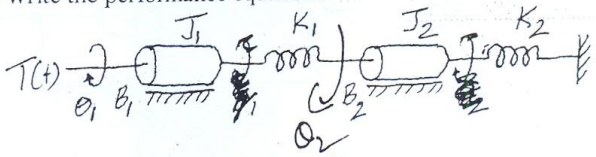

Fig.Q.1(b)

c. Write an explanatory note on gear trains. **(04 Marks)**

2 a. Define the term transfer function of a linear time invariant system. Derive the expression for the transfer function of a closed loop negative feedback system. **(06 Marks)**

b. For the block diagram shown in the Fig.Q.2(b), determine the overall transfer function using block diagram reduction rules. **(06 Marks)**

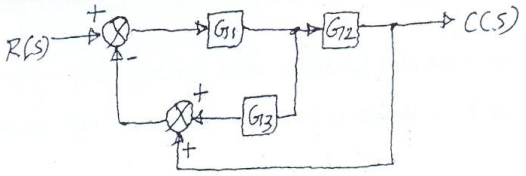

Fig.Q.2(b)

c. Consider the electrical circuit shown in Fig.Q.2(c). Find $\frac{V_0(s)}{V_i(s)}$ using Mason's gain formula. **(08 Marks)**

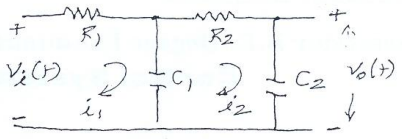

Fig.Q.2(c)

3 a. Define the following terms with respect to an underdamped second order system: i) Peak time; ii) Settling time; iii) Steady state error. **(06 Marks)**

b. A unity feedback system is characterized by an open loop transfer function $G(s) = \frac{K}{s(s+10)}$. Determine the gain K so that the system will have a damping ratio of 0.5. For this value of K, determine settling time, peak over shoot and time to peak overshoot for a unit step input. **(08 Marks)**

c. For a unity feedback system whose open loop transfer function is $G(s) = \frac{50}{(1+0.1s)(1+2s)}$. Find the error constants K_p, K_v, K_a. **(06 Marks)**

4 a. State the Routh's stability criterion and mention its limitation. **(04 Marks)**

b. Consider the characteristic equation $s^6 + 2s^5 + 8s^4 + 12s^3 + 20s^2 + 16s + 16 = 0$. Using Routh's criterion, determine the stability of the system. **(08 Marks)**

c. The closed loop system shown in Fig.Q.4(c) has $G(s) = \frac{K(s+30)}{s(s+5)}$ and $H(s) = \frac{1}{(s+15)}$. Find the range of K for which system is stable. **(08 Marks)**

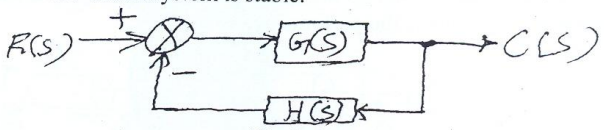

Fig.Q.4(c)

PART – B

5 a. Discuss the various rules for construction of root loci. **(08 Marks)**

b. A negative feedback control system is characterized by $G(s)H(s) = \frac{K}{s(s+1)(s+2)(s+3)}$. Sketch the root locus plot for values of K ranging from 0 to ∞, Mark all the salient points on the root locus. **(12 Marks)**

6 a. Discuss the procedure to evaluate Gain margin and phase margin using Bode plots. **(06 Marks)**

b. Sketch the Bode plot for the transfer function $G(s) = \frac{Ks^2}{(1+0.2s)(1+0.02s)}$. Determine the system gain K for the gain cross over frequency to be 5 rad/sec. **(08 Marks)**

c. For the Bode magnitude asymptotic plot of Fig.Q.6(c), determine the transfer function in frequency domain. **(06 Marks)**

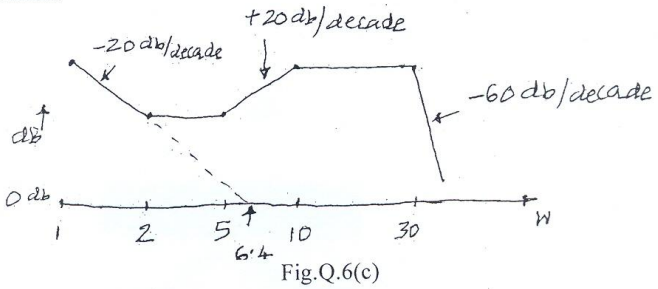

Fig.Q.6(c)

7 a. State the Nyquist stability criterion. **(06 Marks)**

b. Using the Nyquist stability criterion, investigate the stability of a closed loop system whose open loop transfer function is given by $G(s)H(s) = \frac{K}{(s+1)(s+2)}$. **(14 Marks)**

8 a. State the properties of state transition matrix. **(04 Marks)**

b. Represent the electrical circuit shown in Fig.Q.8(b) by a state model. **(08 Marks)**

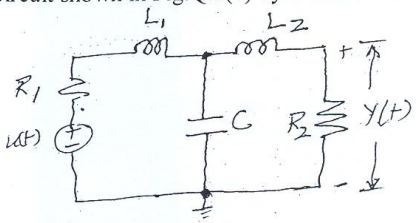

Fig.Q.8(b)

c. For the signal flow graph of Fig.Q.8(c) write the state and output equations: **(08 Marks)**

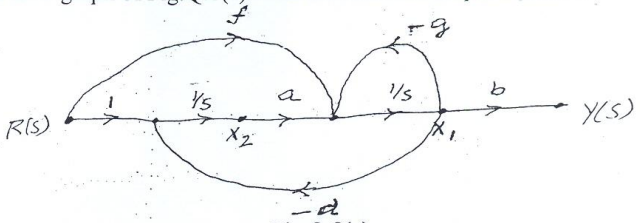

Fig.Q.8(c)

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10EC44

Fourth Semester B.E. Degree Examination, Dec.2016/Jan.2017
Signals and Systems

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Determine and sketch the even and odd parts of the signal show in Fig.Q.1(a). **(05 Marks)**

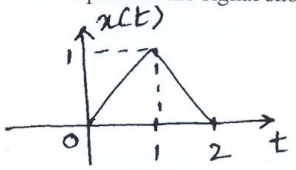

Fig.Q.1(a)

b. Sketch the waveforms of the following signals:
   i) $x(t) = u(t + 1) - 2u(t) + u(t - 1)$
   ii) $y(t) = r(t + 1) - r(t) + r(t - 2)$
   iii) $z(t) = -u(t + 3) + 2u(t + 1) - 2u(t - 1) + u(t - 3)$. **(09 Marks)**

c. For the following system, determine whether the system is: i) Memoryless; ii) Stable; iii) Causal; iv) Linear; v) Time-invariant.
   $y(n) = 2x(n)\, u(n)$. **(06 Marks)**

2 a. Derive the equation for convolution sum. **(05 Marks)**

b. Evaluate the discrete time convolution sum of
   $y(n) = (1/2)^n\, u(n - 2) * u(n)$. **(05 Marks)**

c. Convolve the signals x(t) and h(t) shown below in Fig.Q.2(c). **(06 Marks)**

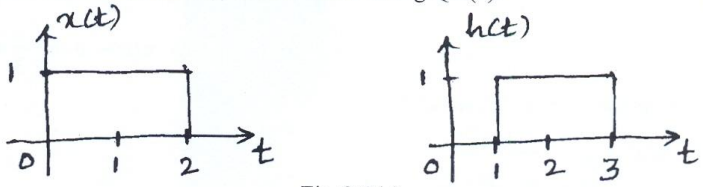

Fig.Q.2(c)

d. Convolve $x(n) = \{1, 2, \underset{\uparrow}{-1}, 1\}$ and $h(n) = \{1, \underset{\uparrow}{0}, 1\}$. **(04 Marks)**

3 a. Find the output, given the input and initial conditions, for the system described by the following differential equation:
   $x(t) = e^{-t}\, u(t)$, $y(0) = -1/2$, $y'(0) = 1/2$, $y''(t) + 5y'(t) + 6y(t) = x(t)$. **(07 Marks)**

b. Determine the forced response for the system described by the following difference equation and the specified input: $x(n) = 2u(n)$, $y(n) - \frac{9}{16}y(n-2) = x(n-1)$. **(07 Marks)**

c. Draw direct form-I and direct form-II implementations of the system described by the difference equation: $y(n) + \frac{1}{4}y(n-1) + \frac{1}{8}y(n-2) = x(n) + x(n-1)$. **(06 Marks)**

4 a. Prove the time shift and frequency shift properties of DTFs. **(06 Marks)**

b. Determine the DTFS of the signal

$$x(n) = \cos\left(\frac{\pi}{3}\right)n .$$ **(06 Marks)**

c. Evaluate the Fourier series representation of the signal $x(t) = \text{Sin } 2\pi t + \cos 3\pi t$. Also sketch the magnitude and phase spectra. **(08 Marks)**

PART – B

5 a. Prove the convolution property of DTFT. **(05 Marks)**

b. Find the DTFT of unit step sequence. **(07 Marks)**

c. Compute the Fourier transform of the signal

$$x(t) = \begin{cases} 1+\cos \pi t; & |t| \le 1 \\ 0; & |t| > 1 \end{cases} .$$ **(08 Marks)**

6 a. The impulse response of a continuous time system is given by

$$h(t) = \frac{1}{RC} e^{-t/RC} u(t) .$$

Find the frequency response and plot the magnitude and phase response. **(05 Marks)**

b. Obtain the FT representation for the periodic signal $\sin w_o t$ and draw the spectrum. **(07 Marks)**

c. Find the DTFT representation for the periodic signal

$$x(n) = \cos\left(\frac{\pi}{3}\right)n$$

Also draw the spectrum. **(05 Marks)**

d. Write a note on sampling theorem and Nyquist rate. **(03 Marks)**

7 a. List the properties of region of convergence. **(05 Marks)**

b. Determine the Z-transform, the ROC, and the locations of poles and zeros of x(z) for the following signals: **(08 Marks)**

i) $x(n) = -\left(\frac{3}{4}\right)^n u(-n-1) + \left(\frac{-1}{3}\right)^n u(n)$ ii) $x(n) = n \sin\left(\frac{\pi}{2}n\right) u(-n)$.

c. Find the inverse Z-transform of

$$X(z) = \frac{1 - z^{-1} + z^{-2}}{\left(1 - \frac{1}{2}z^{-1}\right)\left(1 - 2z^{-1}\right)\left(1 - z^{-1}\right)}$$

with following ROCs i) $1 < |z| < 2$ ii) $\frac{1}{2} < |z| < 1$. **(07 Marks)**

8 a. Find the transfer function and impulse response of a causal LTI system if the input to the system is $x(n) = (-1/3)^n u(n)$ and the output is $y(n) = 3(-1)^n u(n) + (1/3)^n u(n)$. **(08 Marks)**

b. Determine the transfer function and difference equation representation of an LTI system described by the impulse response $h(n) = (1/3)^n u(n) + (1/2)^{n-2} u(n-1)$. **(04 Marks)**

c. Determine the forced response, natural response and output of the system described by the difference equation $y(n) + 3y(n-1) = x(n) + x(n-1)$, if the input is $x(n) = \left(\frac{1}{2}\right)^n u(n)$ and $y(-1) = 2$ is the initial condition. **(08 Marks)**

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10EC45

Fourth Semester B.E. Degree Examination, Dec.2016/Jan.2017
Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. Explain composite VHDL and verilog data types. **(08 Marks)**

b. If A, B and C are the unsigned variables with A = "110011", B = "010100", C = "101". Find the values of
(i) Y = &A (ii) Y = A && B (iii) Y = A sra 2
(iv) Y = B rol 2 (v) Y = A << 2 (vi) Y = A and not B xor 2 nand C **(07 Marks)**

c. Write the major differences between VHDL and verilog. **(05 Marks)**

2 a. Write a VHDL program in data flow style using signal assignment statements to implement a 2 to 1 multiplexer with active low enable signal (Ebar). If the propagation delay of each gate is 9 ns, calculate at what time the output is available when the input signals (A, B, select, Ebar) are changed at T_0, T_1 and T_2 as shown in Fig.Q2(a). **(07 Marks)**

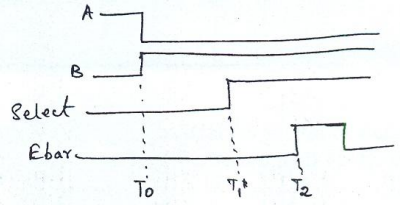

Fig.Q2(a)

b. Write a VHDL program to realize a D-latch in Data flow style, Consider enable signal as active low. **(06 Marks)**

c. Write a verilog program to implement a 3-bit carry-look ahead adder in data flow style. **(07 Marks)**

3 a. Compare signal and variable assignment statement. **(05 Marks)**

b. Write a verilog code to implement a positive edge triggered JK flip flop shown in Fig.Q3(b) in behavioural style using (i) else if and (ii) case statement. **(08 Marks)**

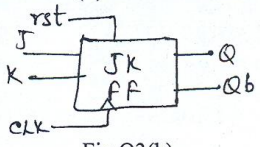

Fig.Q3(b)

c. Write the flow chart of Booth multiplication algorithm. Show the steps to find the product of two signed 5-bit numbers –5 and 9. **(07 Marks)**

4 a. Write a VHDL program to realize the block diagram shown in Fig.Q4(a) in structural style (No need to show the implementation of components). **(07 Marks)**

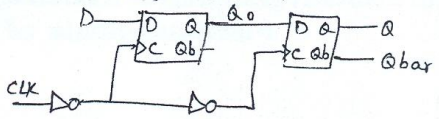

Fig.Q4(a)

b. Write a verilog program to implement a 4-bit magnitude comparator using 4-bit adders in structural style. **(07 Marks)**

c. Explain the following keywords (i) Generate (ii) Generic and (iii) Parameter. **(06 Marks)**

PART – B

5 a. Explain procedure with syntax and example in VHDL. **(06 Marks)**

b. Write a verilog program to convert an unsigned binary to an integer using task. **(08 Marks)**

c. Write a VHDL function to find the greater of two signed numbers. **(06 Marks)**

6 a. When mixed type description is preferred? Give example. **(06 Marks)**

b. Explain different VHDL user defined types. **(06 Marks)**

c. Write a verilog description of a 32×8 SRAM to implement the function table shown in Table 6(c).

CS	R/$\overline{WR}$	Memory Function
0	X	Deselected
1	1	Read cycle
1	0	Write cycle

Table 6(c) **(08 Marks)**

7 a. Explain how to invoke a VHDL entity from a verilog module. **(08 Marks)**

b. Write the block diagram of a 9-bit adder and implement it by mixed language description. **(12 Marks)**

8 a. What is synthesis? With a neat flow chart explain the steps involved in a synthesis process. **(10 Marks)**

b. Find the gate-level mapping for the verilog code given below:

```
module if_st(a, y)
input[2:0] a;
output y;
reg y;
always (a)
  begin
    if (a < 3' b 1 0 1)
      y =1' b 1;
    else
      y = 1' b 0;
    end
end module
```

(10 Marks)

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10EC46

Fourth Semester B.E. Degree Examination, Dec.2016/Jan.2017
Linear ICs and Applications

Time: 3 hrs. Max. Marks:100

Note: *1. Answer any FIVE full questions, selecting atleast TWO questions from each part.*
2. Use of standard resistor value and standard capacitor value table is allowed.

PART – A

1 a. Define the following terms with respect to opamp and specify their typical values for a 741 opamp:
i) CMRR ii) PSRR iii) Slew Rate. **(06 Marks)**

b. Derive an expression for the output voltage of non-inverting summing circuit. **(07 Marks)**

c. The difference of two input signals is to be amplified by a factor of 37. Each input has an amplitude of approximately 50 mV. Using LF353 opamp, design a difference amplifier to obtain approximately equal input resistance at the two input terminals and also provide common mode nulling. **(07 Marks)**

2 a. Using a BIFET opamp, design a capacitor coupled inverting amplifier with an input signal of 30 mV, a load resistance of 2.2 kΩ, $A_V = 150$ and $f_l = 80$ Hz. **(05 Marks)**

b. A high input impedance capacitor coupled non-inverting amplifier is to be designed using 741 opamp with $A_V = 120$, $f_l = 100$ Hz, input signal of 50 mV, and the load resistance ranging from 2.7 kΩ to 27 kΩ. **(09 Marks)**

c. Using 741 opamp with maximum input bias current of 500 nA, design a capacitor coupled voltage follower with a lower cutoff frequency of 120 Hz, and load resistance of 8.2 kΩ using +30V power supply. **(06 Marks)**

3 a. Discuss about the conditions that have to be fulfilled for an opamp circuit to oscillate. **(05 Marks)**

b. With the help of circuit schematic and frequency response, explain how phase lag compensation can be used to stabilize opamp circuit. **(05 Marks)**

c. Mention the need for Z_{in} MOD compensation. Discuss the role of compensating components in Z_{in} MOD compensation for an inverting amplifier. **(05 Marks)**

d. List the precautions to be observed for opamp circuit stability. **(05 Marks)**

4 a. Design a low resistance voltage source (with reference voltage derived from potential divider) to provide an output voltage of 8V. A 741 opamp with a ±15V supply is to be used, and the maximum output current is to be 60 mA. **(08 Marks)**

b. Determine the range of resistance of externally connected resistor R_G for a LH0036 IC instrumentation amplifier to give a voltage gain adjustable from 30 to 300. **(03 Marks)**

c. Design a precision full wave rectifier consisting of a summing circuit and a precision half wave rectifier to produce a 2V peak output from a sine wave input with peak value of 0.5 V and frequency of 1 MHz. Use bipolar opamps with a supply voltage of ±15V. **(09 Marks)**

PART – B

5 a. A ±5V, 10 kHz square wave from a signal source with a resistance of 100 Ω is to have its positive peak clamped precisely at ground level. Tilt on the output is not to exceed 1% of the peak amplitude of the wave. Design the precision clamping circuit using a supply of ±12V. **(08 Marks)**

b. Draw the fundamental circuit of logarithmic amplifier and derive an expression for output voltage. **(06 Marks)**

c. Design a wein bridge oscillator to have an output frequency of 15 kHz using a BIFET opamp with a supply voltage of ±12V. **(06 Marks)**

6 a. With a neat circuit diagram and associated waveforms explain the working principle of inverting Schmitt trigger circuit. **(05 Marks)**

b. Explain the working principle of astable multivibrator with a neat circuit schematic and waveforms. Specify the design procedure for this circuit. **(09 Marks)**

c. Using a 741 opamp, design a second order low pass filter with a cutoff frequency of 1 kHz. **(06 Marks)**

7 a. Discuss about the important characteristics of three terminal IC regulator. **(04 Marks)**

b. Draw the functional block diagram of IC723 voltage regulator and explain. **(06 Marks)**

c. With the help of circuit schematic explain the principle of operation of switched mode power supply. Mention its advantages. **(10 Marks)**

8 a. Draw the circuit diagram of monostable multivibrator using IC 555 and derive the expression for output pulse width. **(05 Marks)**

b. Give the basic block schematic of PLL and explain the function of each block. **(06 Marks)**

c. Draw the functional diagram of dual slope ADC and explain its working principle. Mention its advantages and limitations. **(09 Marks)**

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